Design of a Low Power NoC Router using Marching Memory Through type

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Outline

- **Background.**
- *Marching Memory Through Type (MMTH).*
- Proposed router.
- Evaluation.
- Conclusion.
In many-core chips, NoC consumes significant power

- MIT 16-core RAW CMP: 36%
- Intel 80-core Tera FLOPS: 28%
- Intel 48-core SCC: 10%

Reducing the power of NoCs is essential
Input buffers in routers

- Input buffers in routers consume significant part of the total power of NoCs
  - About 46% of the total power [P. Kundu, Workshop on On- and Off-Chip Interconnection Networks for Multicore Systems’06]
  - The largest leakage power consumer [X. Chen et al., ISLPED’03]
  - Dynamic power is also high and it increases rapidly as the traffic increases [T. T. Ye et al., DAC’02]

- Power optimization of input buffer is required
Various approaches: reduction of the power in buffers

Remove buffers completely
- Buffer-less deflection routers
  - [T. Moscibroda and O. Mutlu, ISCA’09]

Reduce the number of buffers
- Reconfigurable routers
  - [D. Matos, et al., IEEE Transactions on VLSI Systems’11]

Utilize next-generation memory
- A Hybrid buffer design with STT-MRAM
  - [H. Jang, et al., NOCS’12]
Our approach

- Using a novel power efficient buffer memory called Marching Memory Through Type (MMTH) in input buffers

- Complicated buffer management is unnecessary
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What is *Marching Memory*(MM)?

- Novel memory that can avoid the memory bottleneck
- [T. Nakamura and M. J. Flynn, UCAS’10]
- Data are shifted to the CPU synchronized with the clock

**Marching Memory**

- Information/Data marching

1 memory unit marching time = CPU's clock cycle

- Clock
- AND gate with delay

DRAM based memory cell

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An implementation example of the MM concept

The structure and target are completely different from original MM

Not capacitors, but transparent latches
Behavior of MMTH

Write:
- Data are written from the input port to the column indicated by the W-pointer.

Read:
- Data in the column indicated by the R-pointer are transferred to the output port.

MMTH requires some time delay of signals as read latency
A memory cell is composed of a transparent latch. This structure reduces power and area. Simple memory cell. Local clock is unnecessary.
Power consumption of MMTH

- Power consumption depends on data contents
  - If the same bit is written continuously, switching power is not consumed.

- $BCR (Bit \ Change \ Rate)$: Probability of bit change

![Diagram with BCR and power consumption graph]
Summary:
Characteristics of MMTH

**Advantage**
- Low power (68% lower power compared to a bunch of FFs)
- High speed (2GHz)
  - Traditional register-based FIFO: works at only 800MHz

**Disadvantage**
- Read latency (1 clock cycle at 2GHz, 8depth)
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Router architecture

- Standard input-buffered router for 2D mesh
- Virtual-channel flow control (2VCs per input port)

Baseline: a bunch of FFs
Proposed: MMTH
Speculative technique and look-ahead routing are used.

Baseline (using register-based FIFO)  

Naive design with MMTH

Extra Buffer Read stage
Reduction of BR stage

Routing information is stored in an additional temporary flit (pre-header flit)

Pre-header flit arrives at the next router 1 clock earlier than header flit

Diagram:
- Header, Body
- Pre-header
- Bypass buffers
- Producer of BR stage
- Buffer#0
- Buffer#1
- Arbiter
- Crossbar
- NRC

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Proposed router pipeline

Clock cycles

Baseline

1 2 3 4 5 6 7 8 9 10 11 12

Router A

Router B

Router C

MM (naive)

MM (proposed)

Pre-header flit bypasses buffers!
Latency from source to destination

$\text{Latency} = 3H$

$\text{Latency} = 4H$

$\text{Latency} = 3H + 1$

$H$: the number of hops
Additional external signals

- A reset signal
  - Reset MMTH after finishing transmitting a packet

- An invalid signal
  - Invalidate data while BR stage

Invalidate (flit type\(\leq\)none)
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Overview of evaluation

- **Performance**: Cycle-accurate simulation
  - GEM5 full system simulator
  - NAS parallel benchmark
    - A set of programs designed to help evaluate the performance of parallel supercomputers.
    - Derived from computational fluid dynamics applications.

- **Power consumption**: RTL-based simulation
  - Renesas 40nm CMOS design technology
  - Apache Power Artist
    - Synopsys Liberty library format
Simulation setup

(a) CMP System Configuration in GEM5 full system simulator

- Processor: X86-64
- # of processors: 4
- # of directories: 4
- # of L2 caches: 16
- L1 I/D cache size: 32KB
- L2 cache size: 256KB
- Coherence protocol: MOESI directory

(b) NoC System Configuration in RTL models

- Clock frequency: 2GHz
- Topology: 2D-Mesh
- # of cores: 4
- # of VCs/input port: 2
- Buffer size: 8flits
- Routing: XY routing
- Arbiter type: Round-robin
- Flit size: 64bit
- Packet size: 1 header + 6 bodies
- Traffic pattern: Uniform

- 4x4 Mesh
- Each router has a L2 cache bank
- Routers in the four corners are connected with processors and directories
Performance overhead: Network simulation

(a) Uniform random traffic

(b) Bit-complement traffic
Performance overhead: Full system simulation

Baseline
MM(naive)
MM(proposed)

Execution time (Normalized)

Benchmark programs

CG: conjugate gradient

10% 2%

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Bit Change Rate

\[
\text{Power} = P_{\text{min}} + \left( P_{\text{max}} - P_{\text{min}} \right) \frac{\text{BCR}}{100}
\]
Power consumption

The others

Input buffers

Max 45.4%

Ave. 42.4%

Ave. ↑ 13%

Ave. ↓ 68%
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Conclusion

Router using MMTH (a novel power efficient buffer memory) has been presented.

We have compared a router using traditional register-based FIFO and our proposed router.

- It reduces the power consumption by 42.4% on average at 2GHz.
- Performance overhead becomes only 0.5-2.0% by using the proposed mechanism based on look-ahead technique.