Interconnect Enhances Architecture: Evolution of Wireless NoC from Planar to 3D

3D WiNoC Architectures

Hiroki Matsutani
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Outline: Wireless 3D NoC architectures

• Wireless 3D NoCs (3D WiNoCs) [8min]
  – Wireless 3D IC technology
  – 3D WiNoC design example (65nm) [Matsutani, NOCS’11]
  [Miura, IEEE Micro ’13]

• Routing & topology exploration [8min]
  – Spanning tree optimization for irregular WiNoCs
  – Power management via vertical ON/OFF links
    [Matsutani, ASPDAC’13]

• Adding random NoC chip for 3D WiNoCs [5min]
  – Adding randomness induces small-world effects
  – Adding random NoC chip to NoC-less 3D ICs
    [Matsutani, DATE’14]

• Summary [1min]

Hiroki Matsutani, "3D WiNoC Architectures", Special Session at NOCS’14
Design cost of LSI is increasing

- **System-on-Chip (SoC)**
  - Required components are integrated on a single chip
  - Different LSI must be developed for each application

- **System-in-Package (SiP) or 3D IC**
  - Required components are stacked for each application

By changing the chips in a package, we can provide a wider range of chip family with modest design cost
3D IC technology for going vertical

<table>
<thead>
<tr>
<th>Two chips (face-to-face)</th>
<th>Wired</th>
<th>Wireless</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microbump</td>
<td></td>
<td>Flexibility</td>
</tr>
</tbody>
</table>

More than three chips

<table>
<thead>
<tr>
<th>Through silicon via</th>
<th>Scalability</th>
<th>Inductive coupling</th>
</tr>
</thead>
</table>

Wired vs. Wireless
- **Wired**:
  - Microbump
  - Capacitive coupling

- **Wireless**:
  - Flexibility
  - Inductive coupling
Wireless 3D NoC (3D WiNoC)

Three chips are stacked wirelessly

Each router has a wireless transceiver

Each router has TX/RX coils (inductors)

Coils are implemented with metal layers
An example: Cube-1 (2012)

- Test chips for building-block 3D systems
  - **Two chip types:** Host CPU chip & Accelerator chip
  - We can customize number & types of chips in SiP

- Cube-1 Host CPU chip
  - Two 3D wireless routers
  - MIPS-like CPU

- Cube-1 Accelerator chip
  - Two 3D wireless routers
  - Processing element array

[Miura, IEEE Micro 13]
We can change the number and types of chips in a package according to application requirements.
Either vertical P2P links or broadcast bus can be formed for 3D WiNoC

- Vertical point-to-point link between adjacent chips
- Vertical shared bus (broadcast) [Matsutani, NOCS’11]

Either vertical P2P links or broadcast bus can be formed for 3D WiNoC.
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Big picture: Wireless 3D NoC

- Arbitrary chips are stacked after fabrication
  - Each chip has vertical links at pre-specified locations, but we do not know internal topology of each chip
  - Some chips may not have horizontal NoC (vertical link only)

An example (4 chips)
Inductor (vertical link)
Wireless 3D NoC: Up*/down* routing

- Up*/down* (UD) routing
  - Irregular network routing
  - A root node is selected
  - Direction (up or down) is assigned
  - Packets go up and then go down

- Example: 4 chips

The best spanning tree root is selected by exhaustive or heuristic using communication traces (9sec for 64-tile)
Wireless 3D NoC: UD routing w/ VCs

- UD routing with multiple VCs
  - Each layer (VC) has its own spanning tree
  - Packets can transit multiple layers in descent order

You can use either VC0 or VC1

[Koibuchi, ICPP’03]
[Lysne, TPDS’06]
Among 1,000 random topologies, one with the most typical hop count value is selected for the full-system evaluation

- Each tile has router and core (e.g., processor or caches)
- Each horizontal link appears with 50% \((H50)\)
- Each vertical link appears with 100% \((V100)\)
Full-system simulations: Gem5

- **H50-V100 topology** (most typical one among 1,000)
  - Each horizontal link appears with 50% (**H50**)
  - Each vertical link appears with 100% (**V100**)

### Table 1: Simulation parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor architecture</td>
<td>X86-64</td>
</tr>
<tr>
<td>L1$ size &amp; latency</td>
<td>32K / 1cycle</td>
</tr>
<tr>
<td>L2$ size &amp; latency</td>
<td>256K / 6cycle</td>
</tr>
<tr>
<td>Memory size &amp; latency</td>
<td>4G / 160cycle</td>
</tr>
<tr>
<td>Router latency</td>
<td>[BW] [VSA] [ST] [LT]</td>
</tr>
<tr>
<td>Router buffer size</td>
<td>5-flit per VC</td>
</tr>
<tr>
<td>Protocol</td>
<td>MOESI directory (3VC)</td>
</tr>
</tbody>
</table>

### Table 2: Application programs

NPB (BT, CG, EP, FT, IS, LU, MG, SP, UA)

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Full-system simulations: Gem5

- **H50-V100** topology (most typical one among 1,000)
  - Each horizontal link appears with 50% (**H50**)
  - Each vertical link appears with 100% (**V100**)

- The best spanning tree root is selected for each message class (i.e., 3 roots for 3 message classes)

![Graphs showing hop counts for Message class 0 and Message class 1]
Hop count: H50-V100 topology

- Hop count with the worst case spanning tree root
- Hop count with the best case spanning tree root
- Hop count with two spanning tree roots (2 VCs)
- Ideal hop count (not deadlock-free)

Spanning tree optimization always takes the best case.

Spanning tree optimization also improves performance by 12.0% compared to the worst.
App exec time: H50-V100 topology

- H50-V100 w/ the worst case
- H50-V100 w/ the best case
- H100-V100 (all horizontal links available = 3D Mesh)

Spanning tree optimization always takes the best case

Spanning tree optimization improves performance by 12.0% compared to the worst
Energy per flit: H50-V100 topology

- H50-V100 w/ **the worst case** (50% horizontal links)
- H50-V100 w/ **the best case**
- H100-V100 (all horizontal links available = 3D Mesh)

Energy for routers, horizontal links, and vertical links

The next slides will explore vertical ON/OFF links (e.g., H100V50)
Power management: Vertical links

- 5.8mW per 2Gbps channel
- Stop power supply to inductors for low-power
  - "H100-Vn" topology ($n = 100, 50, 25, 15$)
  - Performance/power is improved by spanning tree optimization

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[Image: Power management graph showing TCI power dissipation vs. supply voltage.]

- 5.8mW/channel at 0.92V

[Miura, IEEE Micro 13]

Fujitsu 65nm CMOS

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**Power mgmt: Vertical ON/OFF links**

- **H100-Vn topology** ($n = 100, 50, 25, 15$)
  - All horizontal links are available (**H100**)
  - $(100-n)$% of vertical links are power-gated (**Vn**)
  - Pick up most typical **H100-Vn** among 1,000 trials

---

Chip#3  
Chip#2  
Chip#1  
Chip#0  

**H100-V100**

Chip#3  
Chip#2  
Chip#1  
Chip#0  

**H100-V50**

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**Power mgmt: Vertical off link selection**

- **Random+SPopt (computation cost: low)**
  - Stop \((100-n)\)% of vertical links **randomly**
  - Then, spanning tree optimization is performed to mitigate the performance penalty

- **Exhaustive search (computation cost: HUGE)**
  - Find the least important vertical links and stop them until \((100-n)\)% of vertical links are removed

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**Performance penalty is 2.6% w/ Random+SPopt on H100V50**
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• Summary [1min]

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**Big picture: 3D WiNoC w/ Random**

- Router IP macros have the same # of ports
  - Unused ports can be used for long-range links
- In addition, redundant links can be implemented
  - Statically multiplexed by FPGA-like switch boxes
  - By reconfiguring the switch boxes, an unique random topology is generated

Adding randomness induces small-world effects
Case 1: Random NoC to NoC-less 3D ICs

- Each chip has inductors but does not have 2D NoC
  - Inductors in the same pillar form a **vertical broadcast bus**
  - Horizontal connectivity is not provided at all (i.e., NoC-less)

```
<table>
<thead>
<tr>
<th></th>
<th>Chip#0 NoC-less</th>
<th>Chip#1 NoC-less</th>
<th>Chip#2 NoC-less</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Side view (3 chips)</td>
<td>Chip#2</td>
<td>Chip#1</td>
<td>Chip#0</td>
</tr>
<tr>
<td></td>
<td>Vertical</td>
<td>Vertical</td>
<td>Vertical</td>
</tr>
<tr>
<td></td>
<td>broadcast bus</td>
<td>broadcast bus</td>
<td>broadcast bus</td>
</tr>
</tbody>
</table>
```
Case 1: Random NoC to NoC-less 3D ICs

- Each chip has inductors but does not have 2D NoC
  - Inductors in the same pillar form a **vertical broadcast bus**
  - Adding a **2D Mesh NoC** to such **NoC-less 3D IC**
Case 1: Random NoC to NoC-less 3D ICs

- Each chip has inductors but does not have 2D NoC
  - Inductors in the same pillar form a **vertical broadcast bus**
  - Adding a **Random NoC** to such **NoC-less 3D IC**

![Diagram showing three chips: Chip#0, Chip#1, Chip#2. Chip#0 and Chip#1 are NoC-less, while Chip#2 has a Random NoC. The diagram illustrates the "r-−-" Configuration and a side view of the 3D ICs.]
Case 2: Replacing regular NoC w/ random

- 3D WiNoC that consists of three 2D Mesh NoC layers
  - Inductors in neighboring chips form a **vertical P2P link**
  - E.g., regular 3D Mesh topology (i.e., regular 3D NoC)

![Diagram showing 3D WiNoC with three 2D Mesh NoC layers and vertical point-to-point links between chips.](image_url)
Case 2: Replacing regular NoC w/ random

- 3D WiNoC that consists of three 2D Mesh NoC layers
  - Inductors in neighboring chips form a **vertical P2P link**
  - Replacing **regular 2D Mesh** with **random NoC**
Q1: How many random chips do we need?

Number of random chips vs. Average latency

1 or 2 random chips are enough in the P2P case

1 random chip drastically reduces latency

1 or 2 random chips are enough in the P2P case

1 random chip drastically reduces latency

# of random chips (16-node)  # of random chips (64-node)
Q2: How should we design random chip?

Max. link length (left) & Horizontal degree (right)

Double-length link is enough (equivalent to folded torus)

4 ports are enough (equivalent to 2D mesh/torus)
### Packet latency: P2P (mmmm mrrm rrrr)

<table>
<thead>
<tr>
<th></th>
<th>Mesh</th>
<th>Mesh</th>
<th>Mesh</th>
<th>Mesh</th>
<th>P2P</th>
</tr>
</thead>
<tbody>
<tr>
<td>m m m</td>
<td>Mesh</td>
<td>Mesh</td>
<td>Mesh</td>
<td>Mesh</td>
<td>P2P</td>
</tr>
<tr>
<td>m r r m</td>
<td>Mesh</td>
<td>Rand</td>
<td>Rand</td>
<td>Mesh</td>
<td>P2P</td>
</tr>
<tr>
<td>r r r r</td>
<td>Rand</td>
<td>Rand</td>
<td>Rand</td>
<td>Rand</td>
<td>P2P</td>
</tr>
<tr>
<td>- - - m</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>Mesh</td>
<td>Bus</td>
</tr>
<tr>
<td>- - - r</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>Rand</td>
<td>Bus</td>
</tr>
<tr>
<td>m - - r</td>
<td>Mesh</td>
<td>None</td>
<td>None</td>
<td>Rand</td>
<td>Bus</td>
</tr>
</tbody>
</table>

#### Average packet latency [cycles]

- **mmmm** reduces latency by **20.7%** compared to **mrrr**

![Bar chart showing latency comparison]
---r (adding a random NoC) reduces latency by 26.2% compared to ---m (adding a mesh NoC)
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Summary: 3D WiNoC Architectures

• Inductive-coupling 3D SiP
  – A low cost alternative to build low-volume custom systems by stacking off-the-shelf known-good-dies
  – No special process technology is required; inductors are implemented with metal layers

• Cube-1: A practical 3D WiNoC system
  – Two types: Host CPU chip & Accelerator chips
  – We can customize number & types of chips in SiP
Summary: 3D WiNoC Architectures

- Routing & topology exploration
  - Spanning tree optimization for adhoc 3D WiNoCs
  - Power reduction by **randomly** stopping vertical links
  - Performance/power is improved by spanning tree optimization

- Adding randomness shortens comm. latency
  - Adding **random NoC chip** to **NoC-less 3D ICs**
  - Replacing **regular 2D NoC** with **random 2D NoC**
References (1/2)

• Cube-0: The first real 3D WiNoC

• Cube-1: The heterogeneous 3D WiNoC

• MuCCRA-Cube: Dynamically reconfigurable processor
References (2/2)

• Vertical bubble flow control on Cube-0

• Spanning trees optimization for 3D WiNoCs

• Small-world effects (randomness)
Backup slides