Towards Compelling Cases for the Viability of Silicon-Nanophotonic Technology in Future Many-core Systems

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Acknowledgements: Prof. Davide Bertozzi
Optical On-Chip Communication

For the first time, the photonic elements necessary to build a complete on-chip Optical Communication Infrastructure such as Modulators, Photodetectors, CMOS Drivers and Receivers are today viable for integration on a silicon chip.

- High-speed electro-optic Modulators (10 Gb/s - 40 Gb/s) (85fJ/bit - <25fJ/bit)
- Low-loss waveguides (<1.7dB/cm)
- Broadband routers
- High-efficiency CMOS compatible Photodetectors (40 GHz bandwidths, 1A/W responsivities 1.1 pJ/bit - <50fJ/bit)

Minimum Requirements: <1mW/Gb/s/link @ 1 Tbps/link

Target Platform for chip-scale optical interconnect technology: 3D stacking of processing, memory and optical layers

Sources: IBM, Cornell, Columbia Univ.
Pathfinding

There is currently a huge gap between System Level Designer & Technology Developer

Also, the multi-layer nature of the gap makes compelling cases very difficult to be achieved!!!!!!

Only a cross-layer design methodology can make compelling cases possible and also evolve the ONoC concept into a viable interconnect technology:
- Specification of abstraction layers for ONoC design
- Development of a synthesis methodology
Goal of This Presentation

Today, are we ready to tackle this gap?

A bit of confusion in the Field !!!!

- Descriptive information at different abstraction layers are mixed and hardwired in the same design description.
- Designs are difficult to compare with one another.
- The application of well-known interconnection network techniques is more difficult.
- There are no consistent methodologies to explore the design space.
- Electrical baselines for comparison are naive.
- Technology parameters from different sources.
- Design characterization at high utilization rates.

The goal of this presentation is:

- To systematically define the abstraction layers for ONoC synthesis.
- To specify them for the family of wavelength-routed ONoCs (WRONoCs).
- To highlight the key methodological steps for WRONoC synthesis
- To follow them to augment accuracy of xbenchmarking against an aggressive electrical NoC
Design Methodology for ONoC Synthesis

BEHAVIOURAL MODELING

CHOICE OF THE COMMUNICATION PROTOCOL

TOPOLOGY SELECTION OR SYNTHESIS

PLACE&ROUTE

PHYSICAL DESIGN

(Architecture-Level) NETWORK INTERFACE & PLATFORM INTEGRATION

ELECTRO-OPTICAL NETWORK INTERFACE

TAPE OUT
Design Methodology for ONoC Synthesis

1. Behavioural Modeling
2. Choice of the Communication Protocol
3. Topology Selection or Synthesis
4. Place&Route
5. Physical Design
6. Tape Out

(ARCHITECTURE-LEVEL) NETWORK INTERFACE & PLATFORM INTEGRATION

ELECTRO-OPTICAL NETWORK INTERFACE
Communication Protocols for ONoCs

MOSTLY UTILIZED COMMUNICATION PROTOCOLS

• Space Routing.
• Multiple Writers Single Reader (MWSR).
• Single Writer Multiple Readers (SWMR).
• Multiple Writers Multiple Readers (MWMR).
• Wavelength-Selective Routing.
**BENEFITS**

- No time is spent in Routing/Arbitration.
- Enables Contention-Free Full Connectivity without needing for any path setup/teardown overhead.
- (LIMITED) bit – parallelism can be achieved by either broadband switching or spatial division multiplexing.

**CHALLENGES:** HARD TO SCALE TO A LARGE NUMBER OF COMMUNICATION ACTORS
Design Methodology for ONoC Synthesis

Case study: Wavelength-Routed ONoCs

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PHYSICAL DESIGN

(ARCHITECTURE-LEVEL) NETWORK INTERFACE & PLATFORM INTEGRATION

ELECTRO-OPTICAL NETWORK INTERFACE

TAPE OUT
Network Interface Design: not just E/O and O/E conversion circuitry
Design Methodology for ONoC Design

1. Behavioural Modeling
2. Choice of the Communication Protocol
3. Topology Selection or Synthesis
4. Place & Route
5. Physical Design
6. (Architecture-Level) Network Interface & Platform Integration
7. Tape Out
ASSUMPTIONS

• 4 INITIATORS AND 4 TARGETS (i.e., A, B, C, D).
• INITIATORS USE THE SAME 4 WAVELENGTHS (i.e., 1, 2, 3, 4).
• UTILIZATION OF 1X2 OPTICAL FILTERS.

Overall, 12 1x2 drop filters are needed to realize 16 contention-free optical paths!!!
Let us “cover” the wavelength graph with higher-order switching fabrics (e.g., 2x2 PSEs) in order to obtain logic topologies.

There are precise covering rules for the functional correctness of the topology.

All known WRONoC topologies can be materialized this way!
Meanwhile....Topology Selection

Different wavelength separation/covering methods yield to the known WRONoC topologies

- Multi-stage connectivity pattern vs.
- More or less (MRR) populated grid-like structures vs.
- Wrap-around extensions

<table>
<thead>
<tr>
<th>TOPOLOGY</th>
<th>Total # of MRRs</th>
<th>MAX # of Crossings Logic Scheme</th>
<th>Min(no. of hops)</th>
<th>Higher no. of hops in grids</th>
<th>Less MRR-populated grid</th>
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</thead>
<tbody>
<tr>
<td>8x8 λ-Router</td>
<td>56</td>
<td>7</td>
<td></td>
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<tr>
<td>8x8 GWOR</td>
<td>48</td>
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Design Methodology for ONoC Design

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The Role of the Place&Route Constraints

**Placement Constraints:** It is reasonable to assume that the Hubs are positioned in the middle of the clusters.

Placement Constraints: The Memory Controllers are positioned pairwise at opposite sides of the chip thus reflecting industrial practice (e.g., TILE64).
Layout of the 8x8 Folded Crossbar is much more regular than that of the 8x8 λ-Router and the 8x8 GWOR due to a ring-like structure.

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THE WORST LOGIC TOPOLOGIES HAVE BECOME THE BEST PHYSICAL ONES!!!!!!!
Manual Design vs. Place&Route Tools (PROTON)

- THE CAD TOOL CUTS DOWN ON
  - NUMBER OF CROSSINGS (36 vs. 64)
  - MAX INSERTION LOSS (19 dB vs. 33.3 dB)
  - DESIGN TIME (30 seconds vs. at least 4 days)

Manual Design is clearly error prone and time consuming. Definitely to be avoided when number of initiators & targets scales up!!!!!!!

Place&Route Tools for Optical NoCs are still in their infancy!!
The Optical Ring features a higher degree of design predictability than multi-stage networks in the presence of place&route constraints.

**Target 3D Architecture**

**Physical Layout**

The **Optical Ring** exhibits x3 lower Insertion loss (ILmax) than Multi-Stage ONoC.

PROTON tool used for filter-based topology.
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 TAPE OUT
FABRICATION & TEST CHIP BASED ON SILICON-NANOPHOTONIC TECHNOLOGY

GDSII LAYOUT

ACTUAL PIC (PHOTONICALLY–INTEGRATED –CIRCUIT)

Bit-Error-Rate evaluation @ 10 Gb/s on GWOR(ECOC 2013)
....Challenge me Now!!!!

ONoC vs. ENoC
Let us consider a Tilera-style 4x4 CMP: **1.2 GHz operating speed, 32 bit parallelism** Directory-based implementation of the MOESI protocol

**CASE STUDY**

**Cache-Coherent Multi-Core Platform**

**ENoC: ultra-low cost NoC design point (xpipesLite)**

Real synthesis runs on an industrial low-power SVT 40nm technology library! Clock gating applied!
ONoC Selection and Synthesis

- Behavioural Modeling
  - Choice of the Communication Protocol
  - Topology Selection or Synthesis
  - Place & Route
  - Physical Design
  - Tape Out
- (Architecture-Level) Network Interface & Platform Integration
An abstract ONoC model (i.e., a contention-free all-to-all connectivity fabric) has been integrated into the GEM5 simulation framework (effort led by University of Siena, Italy).

This abstraction layer typically ignores:
- Finite buffer size @ injection/ejection IFs
- Backpressure effects in the interconnect
- Clock resynchronization concerns
- Integration overhead with electronics
- Message-dependent deadlock
- Design predictability gap

Common Risk: overly optimistic results!
We modified the GEM5 simulation framework to more accurately reflect functional and non-functional parameters of the selected ONoC as well as of its network interface.

- **GEM5** made aware of: Ring topology, Finite buffer size and backpressure, Matched latency with RTL
- **P&R-aware** Laser Power Tuning

Collaboration with University of Siena
ONoC technology can actually deliver significant performance speedup!

- Even in cache coherent systems, which are not communication-intensive!

On average the ONoC outperforms the ENoC by about 18% @ 3bit and 23% @ 4bit.
An aggressive optical technology gets closer to the break-even point (about 11.6%, @3bit) WITHOUT ACHIEVING IT!

The static energy cost of the optical network interfaces is higher than (almost 2 times @3bit) that of the ONoC.
A good interconnect fabric implies that it is a small contributor to total system energy. An interconnect fabric speeding up application execution causes the system to burn less energy.

**ASSUMPTIONS**

- The Electronic Tile-based Architecture burns **15 Watts**.
- **3 and 4bit parallelism** for ONoC.
- Both **AGGRESSIVE AND CONSERVATIVE** technologies.

**Normalized System Energy**

ENoC

ONoC (Conservative)

ONoC (Aggressive)

- **3 bit**
- **4 bit**

ONoC makes the system more energy efficient even with a conservative technology of optical components.
Conclusions

We highlighted the key methodological steps for the design of a network-on-chip with the emerging nanophotonic technology.

- similar steps to electronic NoCs
- But with different meaning, constraints.....
  .....hence calling for different objective functions, algorithms, tools!
- Most tools needed for an automated design flow are not there yet

Through successive refinements of the design abstractions, we synthesized a WRONoC for accurate comparison against an aggressively low-power ENOC in a target CMP

✓ The superior performance speedups of the ONoC enable the system as a whole to burn power for a lower amount of time.
✓ Energy break-even with the ENoC is still far-away....
✓ ...Energy savings for the system as a whole are already there, even with a conservative silicon photonics technology!
ACKNOWLEDGEMENTS

- This work has been supported by the PHOTONICA project under the “FIRB-Futuro in Ricerca” program, funded by the Italian Government.

- This work would like to thank all authors: Alberto, Hervè, Paolo, Anja, Marta, and also all researchers who joined the project:

  **Coordinator:** Davide Bertozzi (University of Ferrara, Italy).
  **Partner:** Gaetano Bellanca (University of Ferrara, Italy).
  **Partner:** Alberto Parini (University of Ferrara, Italy).
  **Partner:** Giovanna Calò (Politecnico of Bari, Italy).
  **Partner:** Sandro Bartolini (University of Siena, Italy).

- Professor Luca Carloni (Columbia University)

THANKS TO EVERYONE!