A Loosely Synchronizing Asynchronous Router for TDM-Scheduled NOCs

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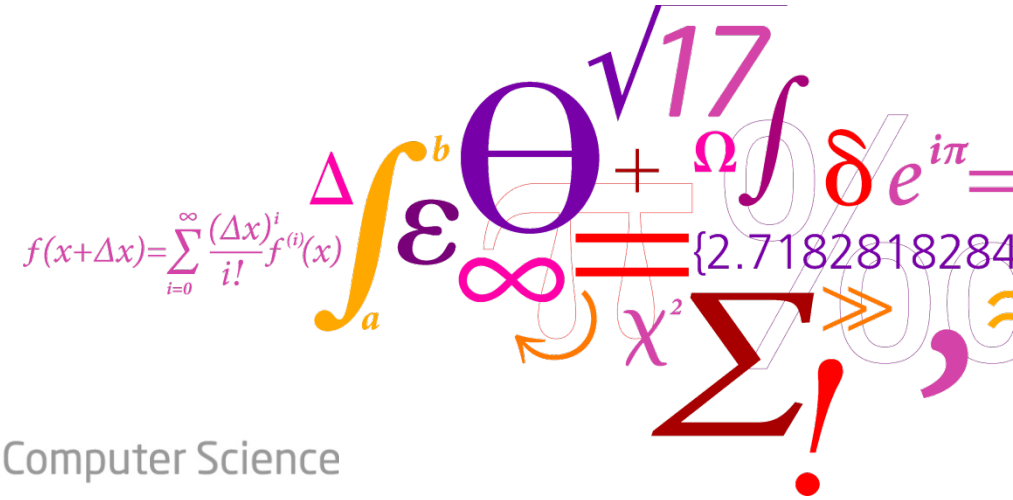

DTU Compute
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Outline

1. Context
2. Background
   - Review of TDM router designs

     Synchronous → Mesochronous → Asynchronous →
3. The new loosely synchronizing Asynchronous router
   - Principle
   - Design
4. Implementation
   - The click-element template (only DFFs and logic)
   - Key click-element components (the conditional fork)
   - Router implementation
5. Results
6. Conclusion

Context

- Two research projects
  - T-CREST
    Time-predictable Multi-Core Architecture for Embedded Systems
    EU FP7 STREP-project (grant no. 288008)
  - RTEMP
    Hard Real-Time Embedded Multiprocessor Platform
    Danish Council for Independent Research | Technology and Production Sciences, Project no. 12-127600
- Multi-Core platforms for real-time systems
  - Focus on WCET
- Research topics
  - Processor architecture
  - Memory hierarchy and memory NOC
  - Message passing NOC
  - Compiler

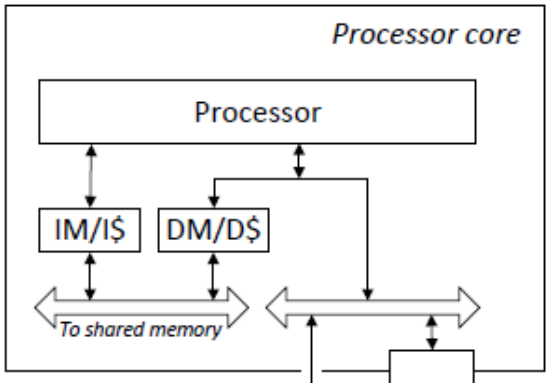
Context

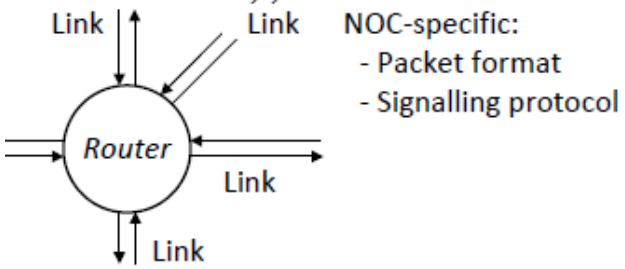
- **Real-time / WCET** → Guarantees on bandwidth and/or latency
  - (Virtual) circuits
    Statically scheduled Time-Division-Multiplexing
    - Nostrum [KTH, Jantsch, Millberg]
    - Æthereal, aelite, daelite, … [TU/e, Goossens, Hansson, …]
  - Non-blocking routers with a rate-control
    - MANGO [DTU, Bjerregaard 1995]

- **Router complexity:**
  - Synchronous aelite: 1
  - Mesochronous aelite: 2
  - Asynchronous MANGO: 10 (buffers, arbitration, flow-control)

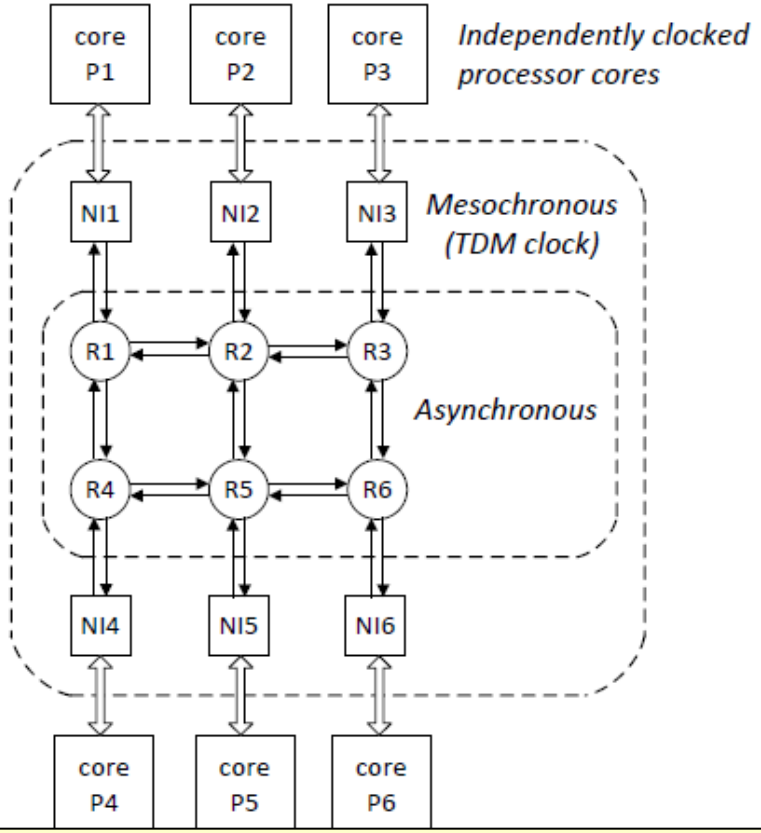
- **GALS (globally synchronous locally asynchronous)**
  - Mainly a requirement to the NOC
    - Mesochronous NOC (clock domain synchronization)
    - Asynchronous NOC

The Argo asynchronous TDM-based NOC



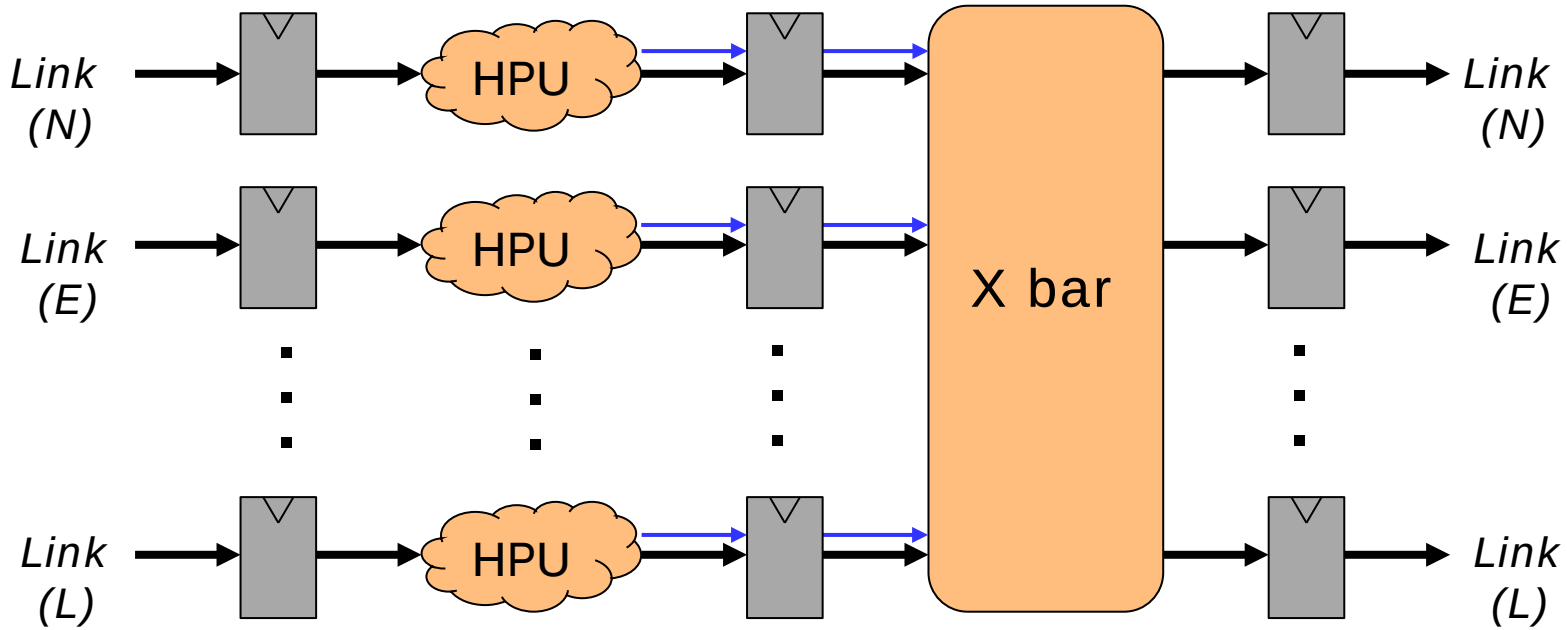


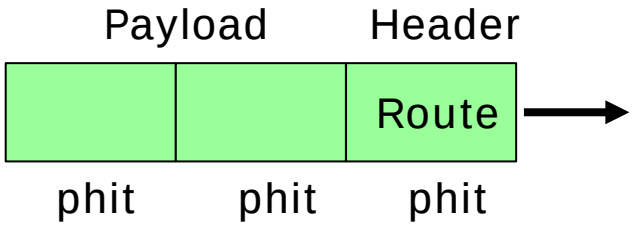
NOC-specific:
- Packet format
- Signalling protocol



Static scheduling and TDM:	Schoeberl at al. NOCS 2012
Router design:	Kasapaki, et al. Euromicro 2013
NI design:	Sparsø, et al. DATE 2013
Timing analysis:	Kasapaki and Sparsø, ASYNC 2014
Scheduler:	Sørensen et al. SEUS 2014

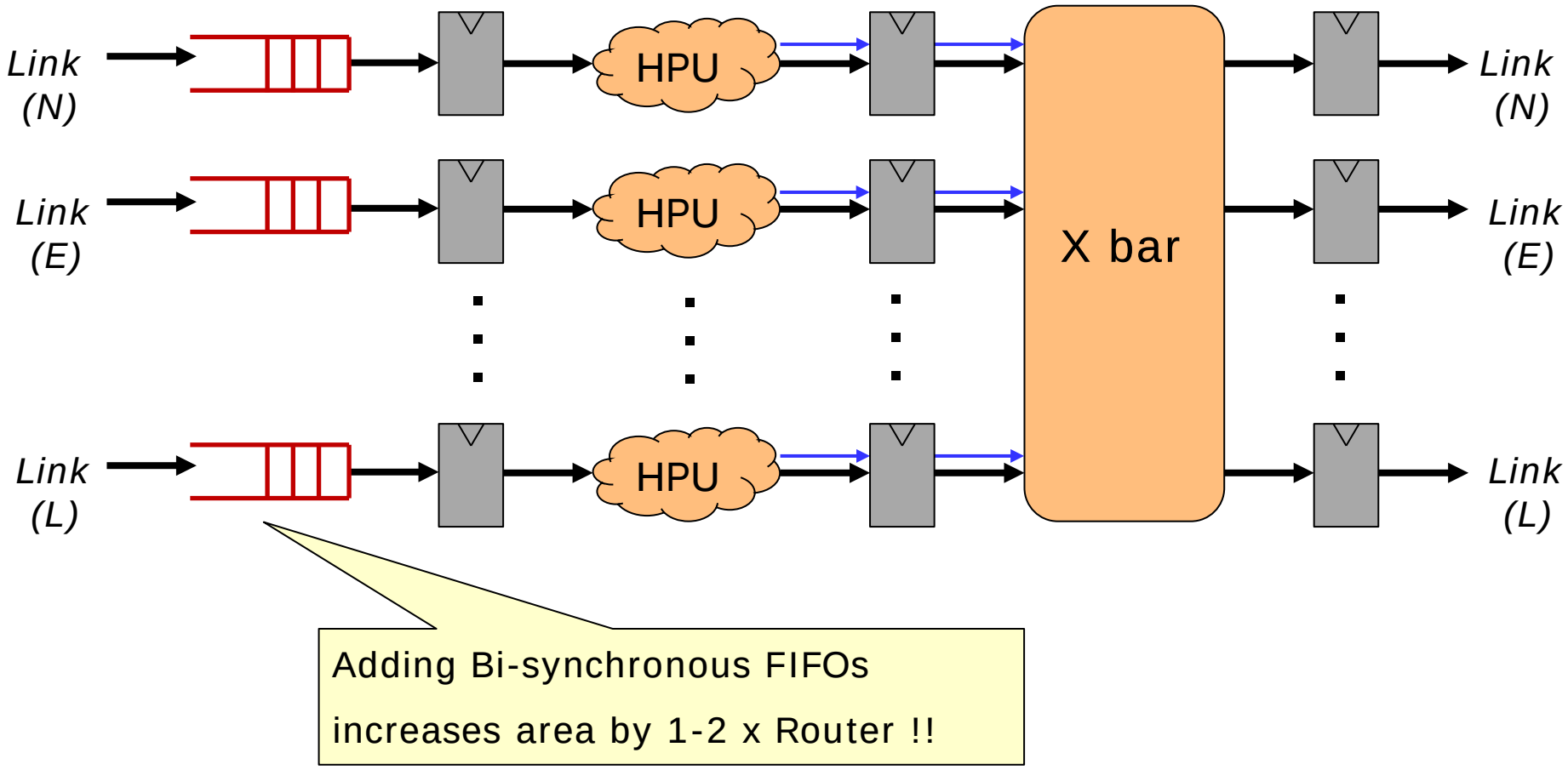
Synchronous TDM router



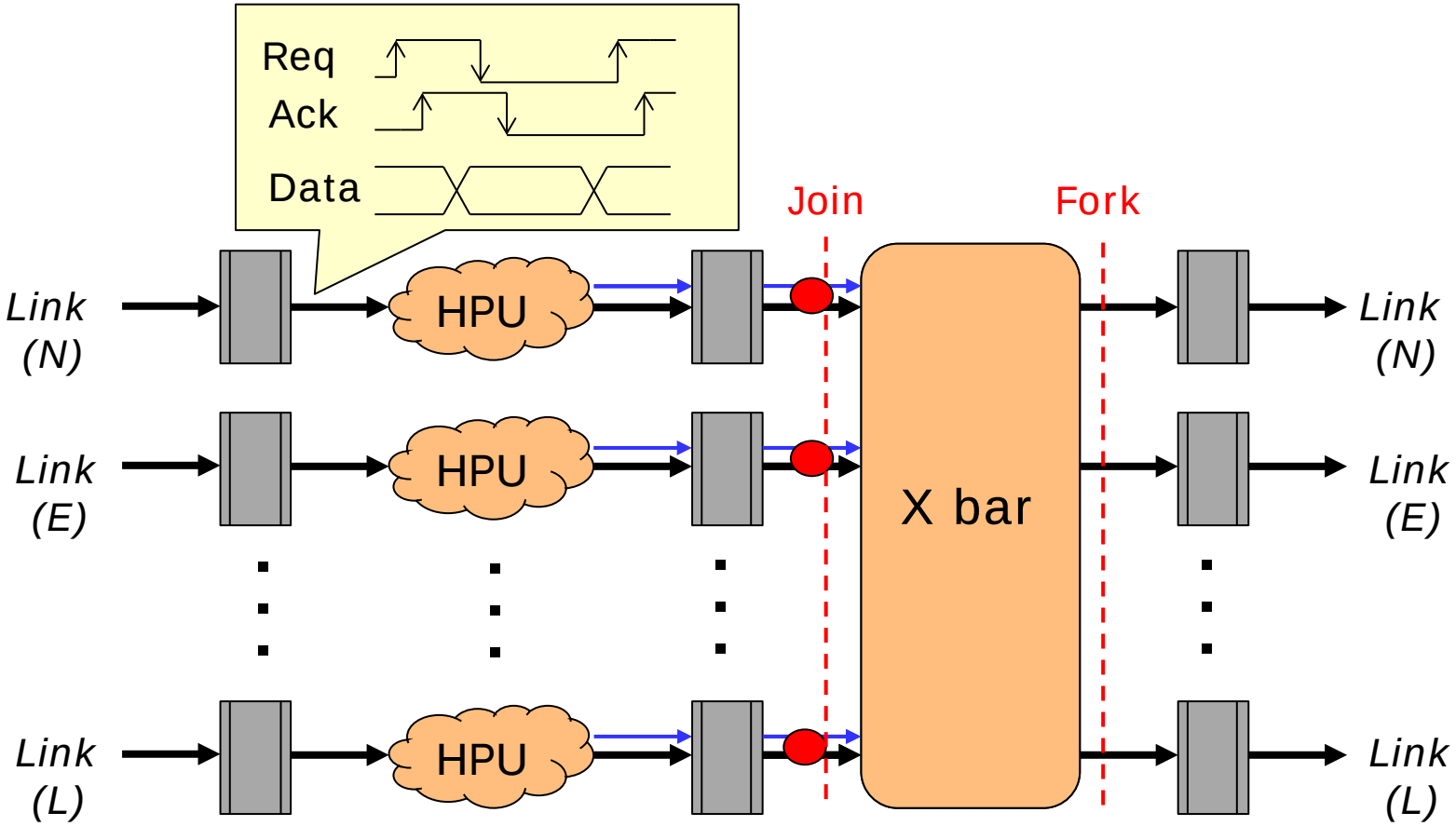


A. Hansson, M. Subburaman, K. Goossens, "Aelite: A Flit-Synchronous Network on Chip with Composable and Predictable Services," DATE 2009

Mesochronous TDM router



Asynchronous TDM router

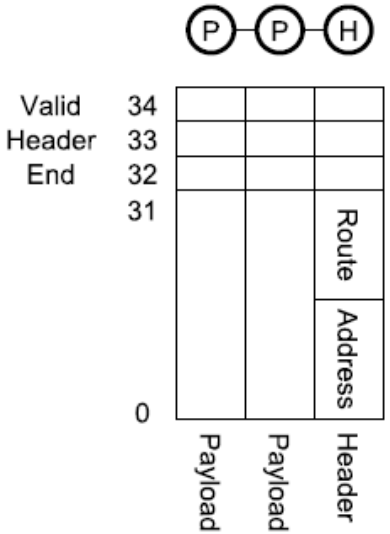


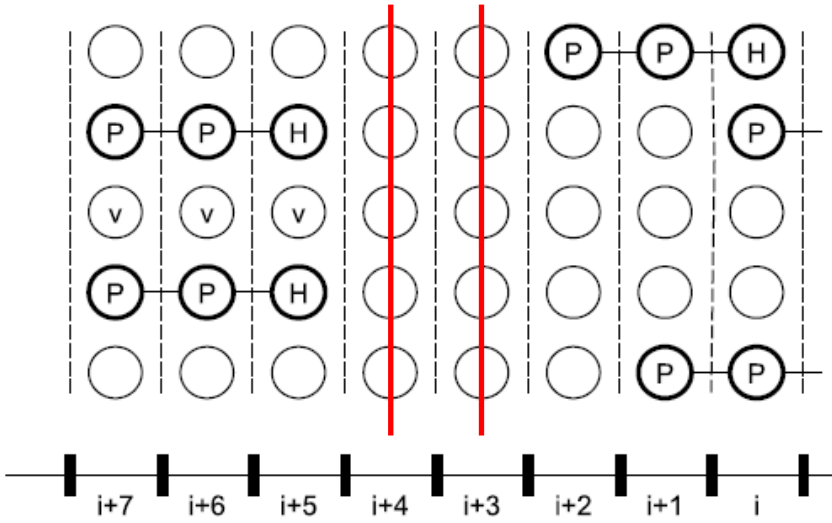
Join-Fork principle briefly mentioned in:

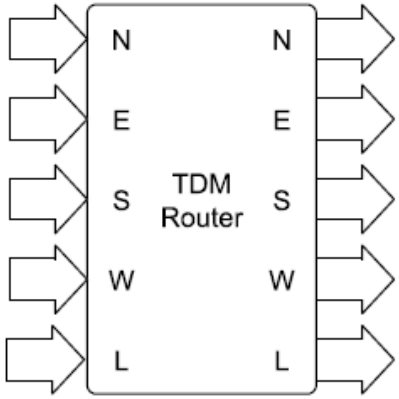
K. Goossens and A. Hansson “The Aethereal Network on Chip after Ten Years: Goals, Evolution, Lessons, and Future”. DAC 2010.

No real implementation of a NOC. Timing behaviour of a network of routers is non-trivial.

The loosely synchronizing router - Principle







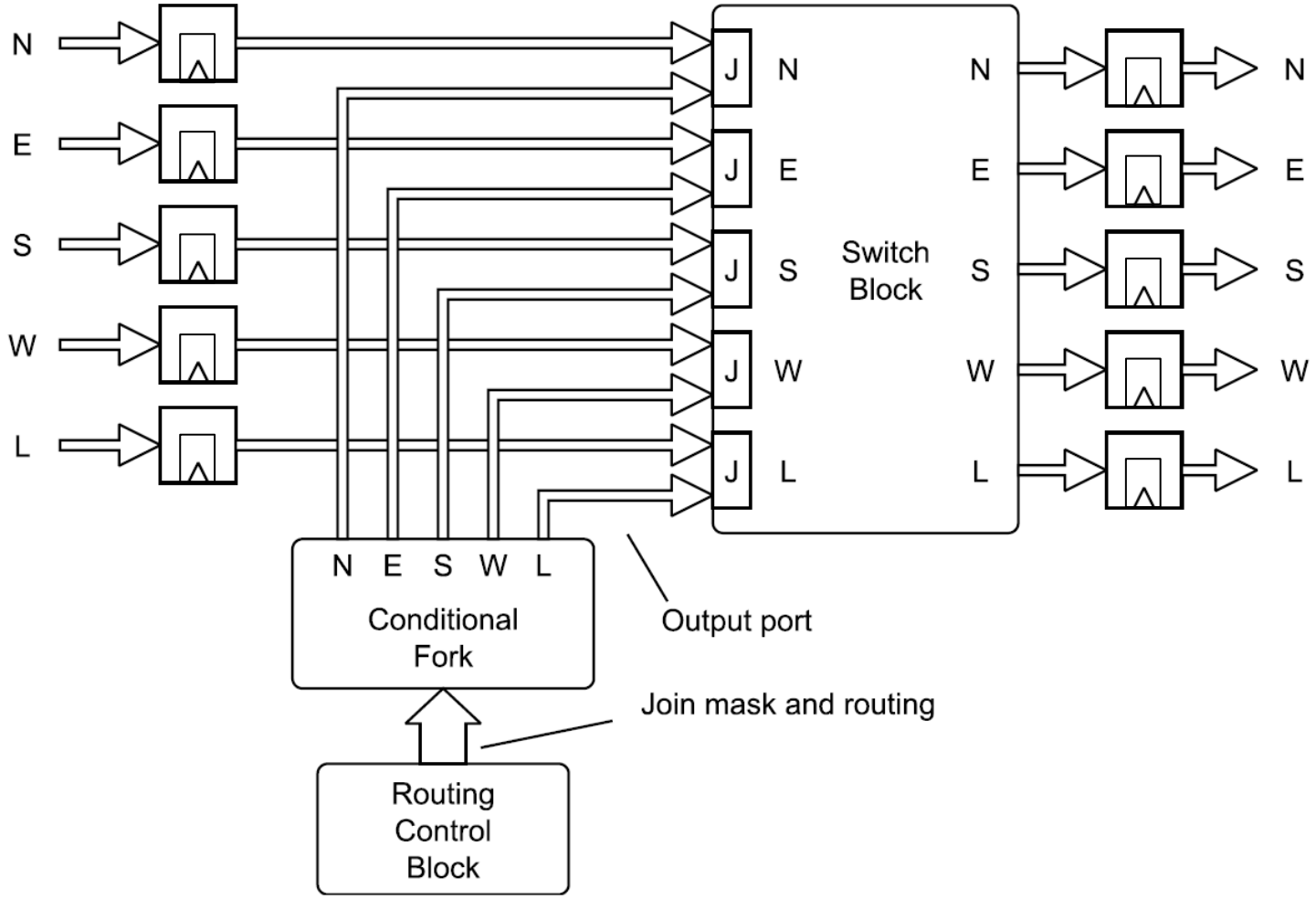
P P H Valid phits (scheduled, slots used) *Full switching*

V Void phit (scheduled, slot not used) *Clock gating*

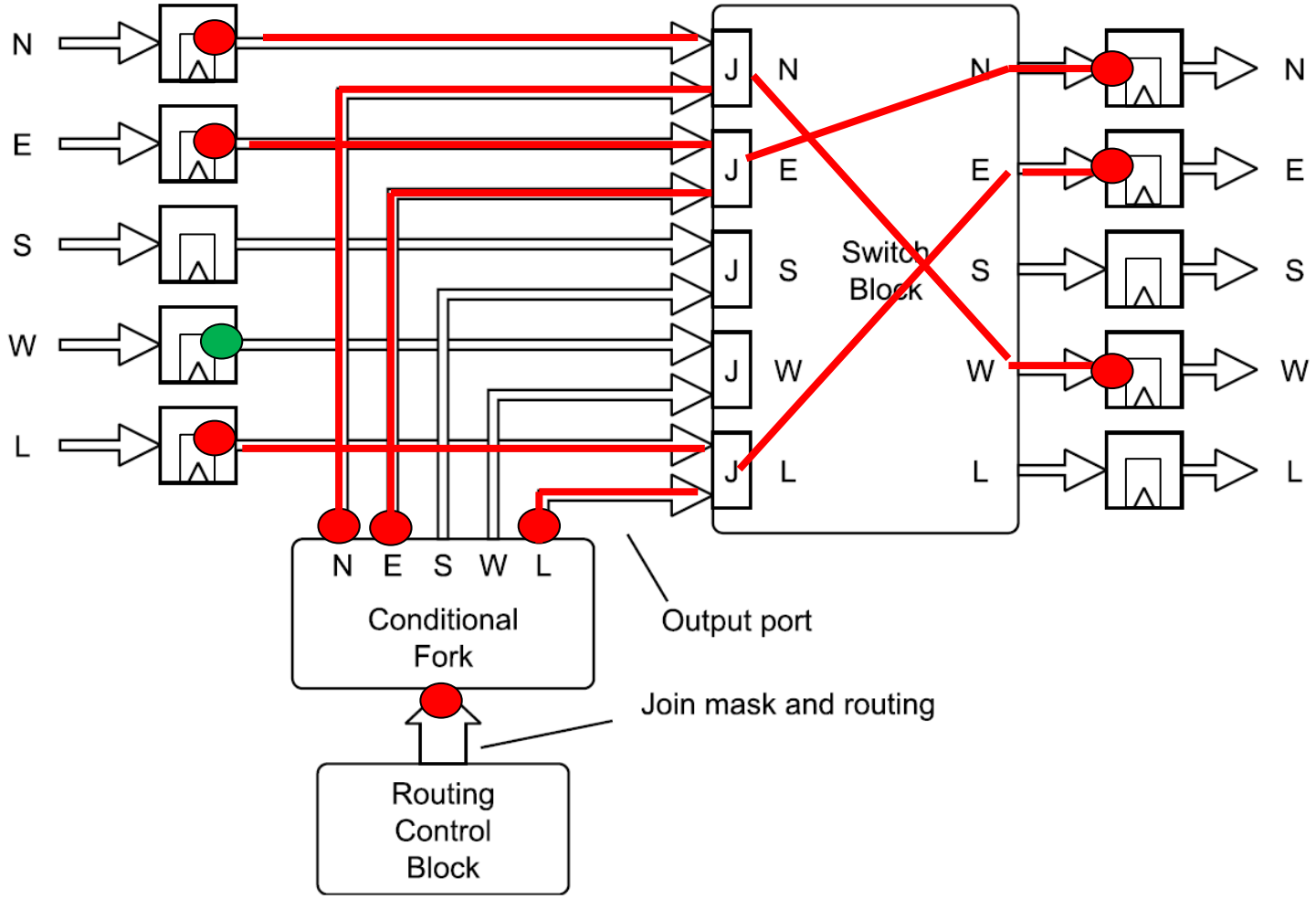
Idle phit (nothing scheduled) ~~*Clock gating*~~

Keep links and router ports silent

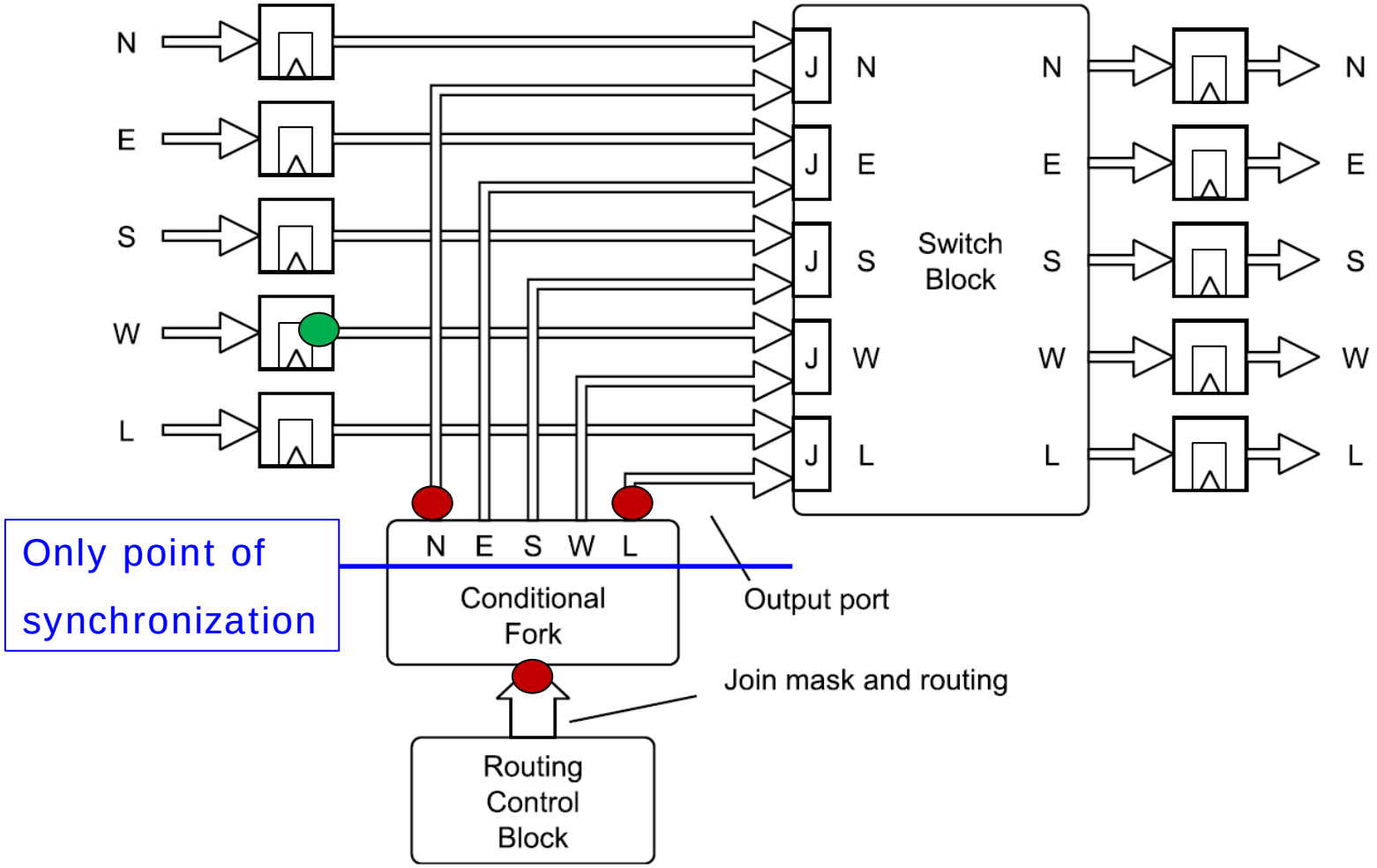
Loosely synchronizing asynchronous router design



Loosely synchronizing asynchronous router design



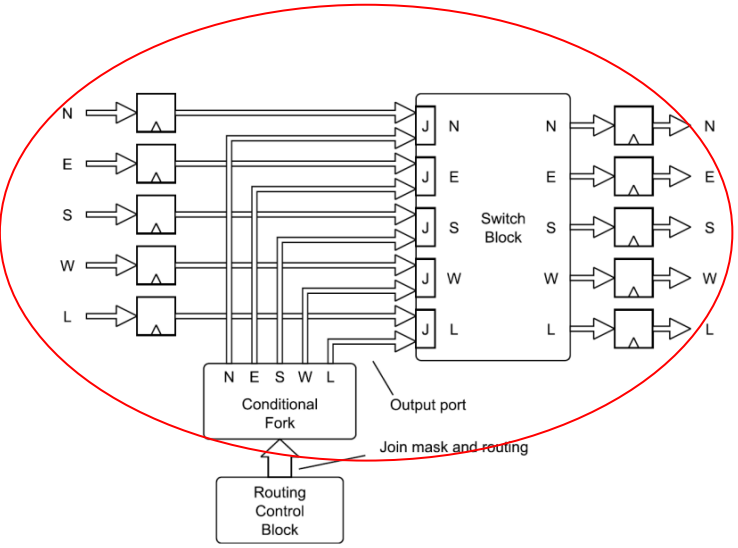
Loosely synchronizing asynchronous router design

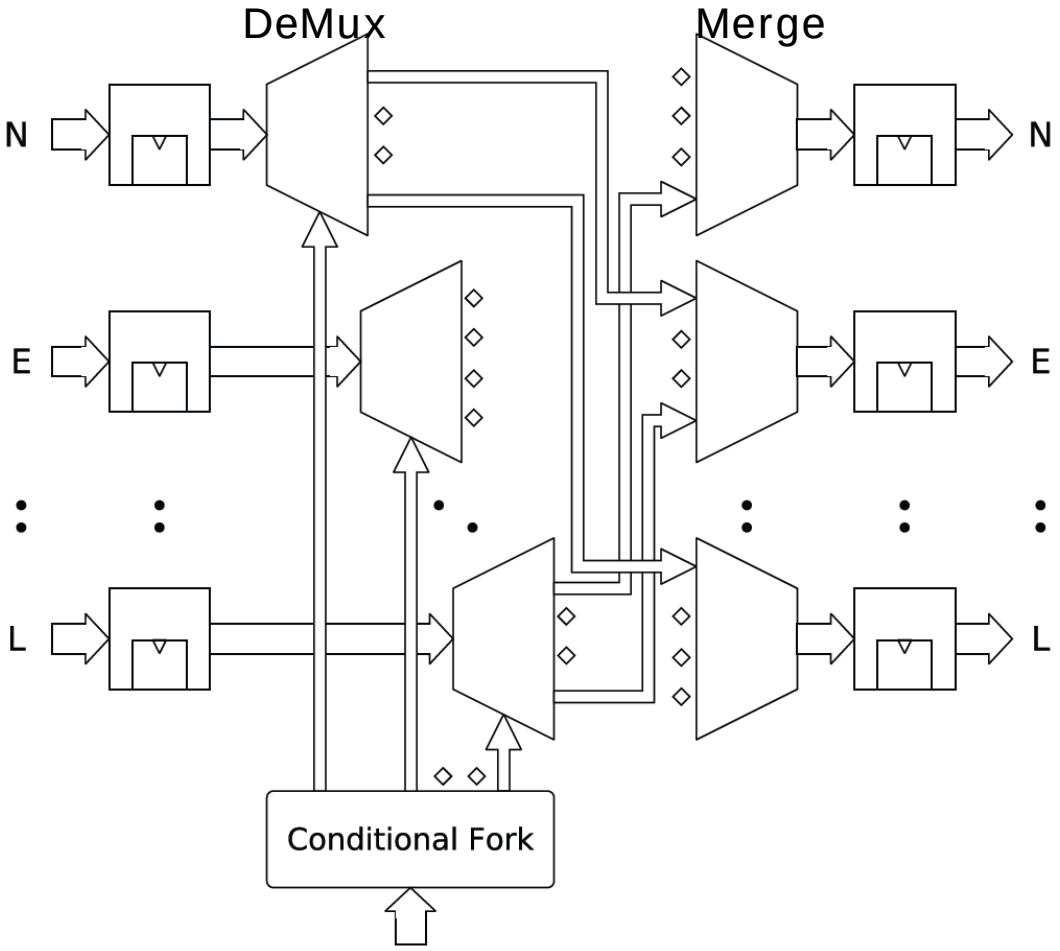


Loose synchronization

- Only local ordering of slots
  - For each individual router
  - For each individual Router-NI-port
- Duration of slots is elastic
- Ordering at Router-NI ports can be influenced by NI interface design.

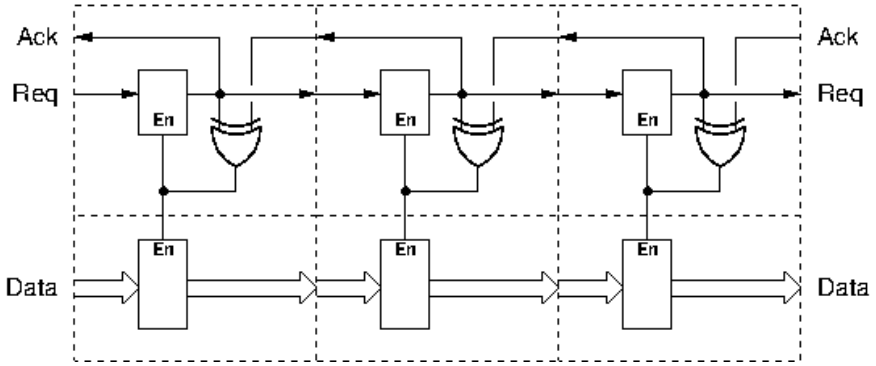
Loosely synchronizing router design





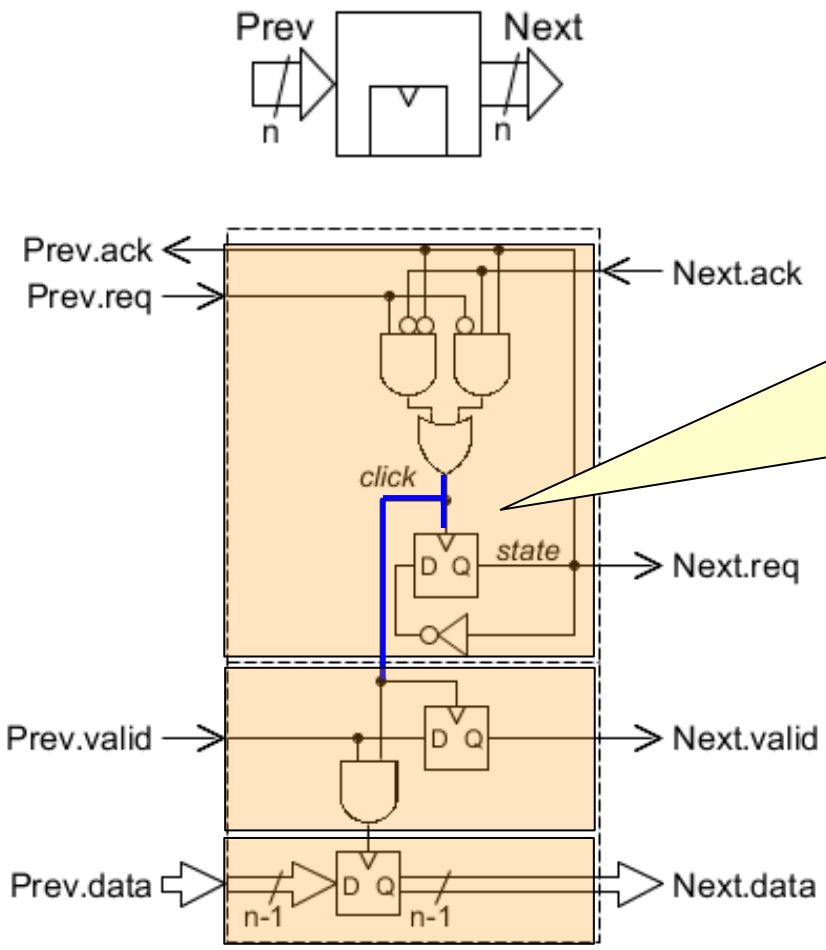
Implementing asynchronous circuits

- Intensive use of C-elements and transparent latches
- Mousetrap pipeline (two-phase bundled-data). [18] Singh and Nowick



  - Timing constraints are tricky to handle in EDA-tools
  - Std. cell library has no latches that reset to “1”.
  - Clock-gating of normally transparent latches is sort of nonsense.
- Click elements (two-phase bundled-data)
  - Ad Peeters et al. ASYNC 2010 [3]
  - Handshake Solutions Inc. stopped its activities soon after ASYNC 2010 paper
  - Uses only edge triggered flip-flops and combinational gates.
  - All signal paths start and end in flip-flops.

Click element based asynchronous design - a handshake register w. gating



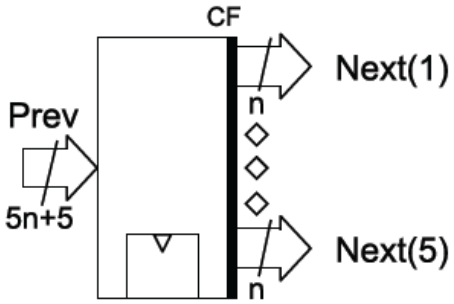
Click 0->1
when
- new data is available from the predecessor

and

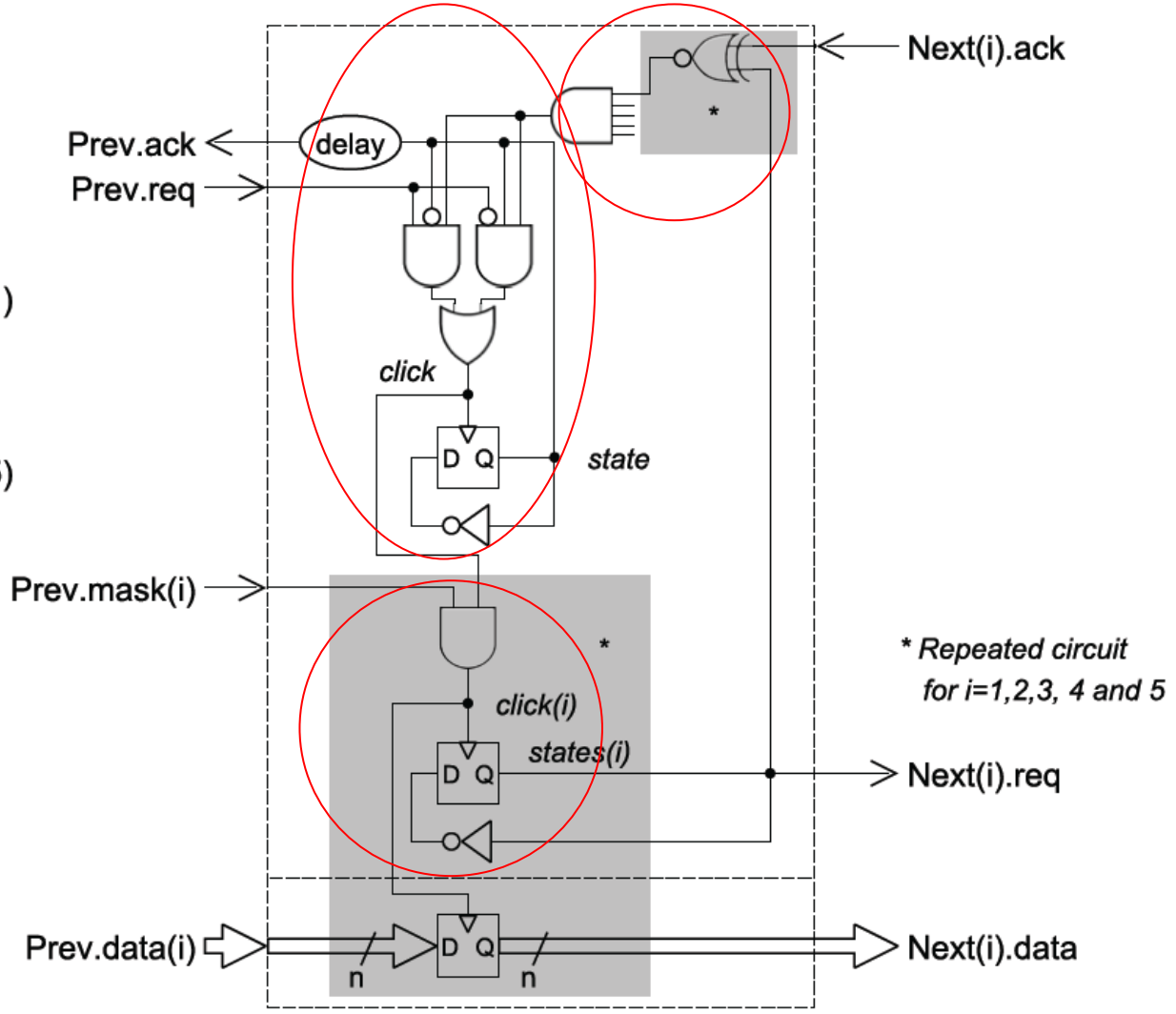
- successor has acknowledged reception of the current data

Click 1->0
after latency of FF→AND→OR

The buffered conditional fork



A handshake on the "Prev" channel causes a handshake on one or more of the "Next(i)" channels.



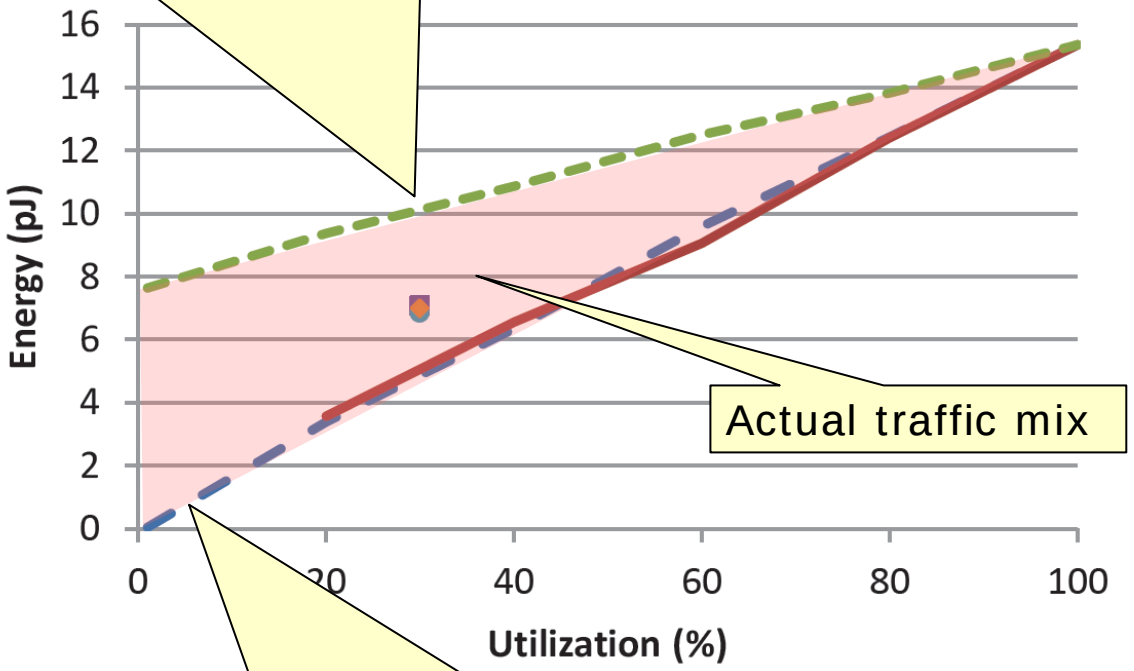
Implementation results.

	Cell area um2	Cycle time ps	Energy per cycle
The new router (65 nm)	36870		
Router control	28890		
Router itself	7980	1150	0 – 15.4 pJ / cycle
Kasapaki [17] (65 nm)	7516	885	1.78 – 8.24 pj / cycle
Ghribaldi [20] (40 nm)	4691	915	2.3 pJ / phit

Energy per cycle (phit-slot)

All slots on all ports reserved. U% are valid phits.

Others are voids. Clock gating saves power



Actual traffic mix

Router is fully utilized in U% of the time slots and otherwise all 5 ports are idle.

Conclusion

- Contributions
  - Shown that TDM can be implemented with very relaxed synchrony.
  - An asynchronous router design that implements this.
  - Explored asynchronous design using click-elements.
  - Implemented of a number of new click-element handshake components.