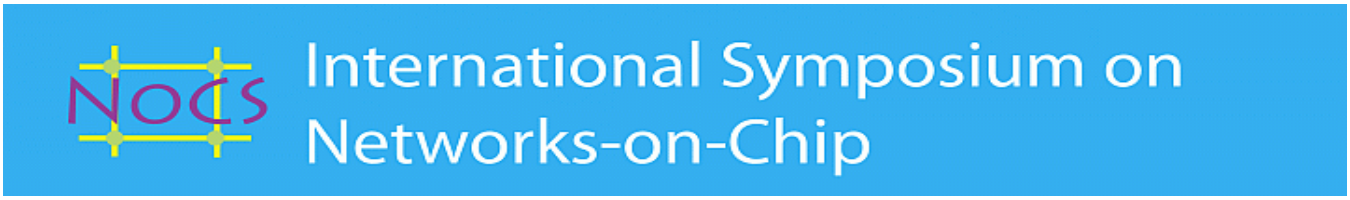

8th IEEE/ACM International Symposium on Networks-on-Chip
September 17th – 19th, 2014
Ferrara, Italia

PROGRAM

WEDNESDAY, SEPTEMBER 17TH, 2014

08.00 – 08.45 REGISTRATION

08.45 – 09.00 OPENING AND WELCOME

09.00 – 10.00 KEYNOTE ADDRESS

High-Performance Energy-Efficient NoC Fabrics: Evolution and Future Challenges

Mark A. Anders, Circuit Research Lab – Intel (USA)

10.00 – 11.00 PAPER SESSION 1

NoC ARCHITECTURE I

1.1 **Single-Cycle Collective Communication Over A Shared Network Fabric**
Tushar Krishna, Li-Shiuan Peh
MIT

1.2 **Extending Bufferless On-Chip Networks to High-Throughput Workloads**
Hanjoon Kim, Changhyun Kim, Miri Kim, Kanghee Won, John Kim
KAIST

11.00 – 11.30 COFFEE BREAK

11.30 – 13.00 PAPER SESSION 2

NoC ARCHITECTURE II

2.1 **An Efficient Network-on-Chip (NoC) Based Multicore Platform for Hierarchical Parallel Genetic Algorithms**
Yuankun Xue[1], Zhiliang Qian[2], Guopeng Wei[3], Paul Bogdan[4], Chi-Ying Tsui[2], Radu Marculescu[3]
[1]Fudan University, [2]The Hong Kong University of Science and Technology, [3]Carnegie Mellon University, [4]University of Southern California

2.2 **Achieving Balanced Buffer Utilization with a Proper Co-Design of Flow Control and Routing Algorithm**
Dong Xiang[1], Miguel Gorgues Alonso[2], Josè Flich[2], José Duato[2]
[1]Tsinghua University, [2]Universidad Politécnica de Valencia

2.3 **FMEA-Based Analysis of a Network-on-Chip for Mixed-Critical Systems**
Eberle A. Rambo, Alexander Tschiene, Jonas Diemer, Leonie Ahrendts, Rolf Ernst
Technische Universität Braunschweig

13.00 – 14.30 LUNCH

14.30 – 16.00 EMBEDDED TUTORIAL

OpenSoC: a Flexible, Parameterizable, Open NoC Generation Tool

Organizers:
Farzad Fatollahi-Fard, Lawrence Berkeley National Laboratory
David Donofrio, Lawrence Berkeley National Laboratory
George Michelogiannakis, Lawrence Berkeley National Laboratory

16.00 – 16.30 COFFEE BREAK

16.30 – 18.30 PAPER SESSION 3
MODELING AND ANALYSIS

3.1 Sampling-Based Approaches to Accelerate Network-on-Chip Simulation
Wenbo Dai, Natalie Enright Jerger
University of Toronto

3.2 An Analytical Model for Worst-case Reorder Buffer Size of Multi-path Minimal Routing in NoCs
Gaoming Du[1], Miao Li[1], Zhonghai Lu[2], Minglun Gao[1], Chunhua Wang[3]
[1]Institute of VLSI Design, Hefei University of Technology, [2]KTH Royal Institute of Technology, [3]School of Microelectronics, Hefei University of Technology

3.3 Transient Queuing Models for Input-Buffered Routers in Network-on-Chip
David Oehmann, Erik Fischer, Gerhard Fettweis,
Technische Universität Dresden

3.4 Towards Stochastic Delay Bound Analysis for Network-on-Chip
Zhonghai Lu[1], Yuan Yao[1], Yuming Jiang[2]
[1]KTH Royal Institute of Technology, [2]Norwegian University of Science and Technology (NTNU)

18.30 CLOSING

THURSDAY, SEPTEMBER 18TH, 2014

EMERGING TECHNOLOGY MORNING

08.30 – 09.45 SPECIAL SESSION 1
SILICON PHOTONIC INTERCONNECTS: AN ILLUSION OR A REALISTIC SOLUTION?
Organizers:
Jiang Xu – Hong Kong University of Science and Technology
Sébastien Le Beux – Lyon Institute of Nanotechnology Yvain Thonnart – CEA LETI

SS1.1 Technology Assessment of Silicon Interposers for Manycore SoCs: Active, Passive, or Optical?
Yvain Thonnart
CEA-Leti, France

SS1.2 Towards Compelling Cases for the Viability of Silicon-Nanophotonic Technology in Future Manycore Systems
Luca Ramini[1], Hervè Tatenguem Fankem[1] , Alberto Ghiribaldi[1], Paolo Grani[2], Marta Ortìn Obòn[4], Anja Boos[3], Sandro Bartolini[2].
[1]University of Ferrara [2]University of Siena [3]TU Munich [4]University of Zaragoza

SS1.3 CLAP: a Crosstalk and Loss Analysis Platform for Optical Interconnects
Mahdi Nikdast[1], Luan H. K. Duong[1], Jiang Xu[1], Sébastien Le Beux[2], Xiaowen Wu[1], Zhehui Wang[1], Peng Yang[1], and Yaoyao Ye[1]*
[1]Hong Kong University of Science and Technology, [2]Lyon Institute of Nanotechnology

09.45 – 11.00 SPECIAL SESSION 2
INTERCONNECT ENHANCES ARCHITECTURE: EVOLUTION OF WIRELESS NoC FROM PLANAR TO 3D
Organizers:
Radu Marculescu – Carnegie Mellon University

Partha Pratim Pande – Washington State University
Deukhyoun Heo – Washington State University
Hiroki Matsutani – Keio University

SS2.1 Foundations of On-chip Communication: Performance and Power Management in 2D and 3D Multicore Platforms
Radu Marculescu
Carnegie Mellon University

SS2.2 Planar WiNoC Architectures
Partha Pratim Pande
Washington State University

SS2.3 3D WiNoC Architectures
Hiroki Matsutani
Keio University

11.00 – 11.30 COFFEE BREAK

11.30 – 13.00 PAPER SESSION 4
OPTICAL NoCs

4.1 Augmenting Manycore Programmable Accelerators with Photonic Interconnect Technology for the High End Embedded Computing Domain
Marco Balboni[1], Marta Ortín Obón[2], Alessandro Capotondi[3], Alberto Ghiribaldi[1], Herve Tatenguem Fankem[1], Luca Ramini[1], Víctor Viñals[2], Andrea Marongiu[4], Davide Bertozzi[1]
[1]University of Ferrara [2]University of Zaragoza [3]University of Bologna [4]University of Bologna, ETH Zurich

4.2 QuT: A Low-Power Optical Network-on-Chip
Parisa Khadem Hamedani[1], Natalie Enright Jerger[1], Shaahin Hessabi[2]
[1]University of Toronto, [2]Sharif University of Technology

4.3 Sharing and Placement of On-chip Laser Sources in Silicon-Photonic NoCs
Chao Chen, Tiansheng Zhang, Pietro Contu, Jonathan Klamkin, Ayse Coskun, Ajay Joshi
Boston University

13.00 – 14.30 LUNCH

14.30 – 16.30 PAPER SESSION 5
LOW POWER NoC

5.1 Variable-Width Datapath for On-Chip Network Static Power Reduction
George Michelogiannakis, John Shalf
Lawrence Berkeley National Laboratory

5.2 Dynamic Synchronizer Flip-Flop Performance in FinFET Technologies
Mark Buckler[1], Arpan Vaidya[2], Xiaobin Liu[2], Wayne Burleson[1]
[1]University of Massachusetts Amherst, AMD Research [2]University of Massachusetts Amherst

5.3 Design of a Low Power NoC Router using Marching Memory Through type
Ryota Yasudo[1], Takahiro Kagami[1], Hideharu Amano[1], Yasunobu Nakase[2], Masashi Watanabe[2], Tsukasa Oishi[2], Toru Shimizu[2], Tadao Nakamura[1]
[1]Keio University [2]Renesas Electronics Corp.

5.4 Bubble Sharing: Area and Energy Efficient Adaptive Routers using Centralized Buffers
Syed Minhaj Hassan, Sudhakar Yalamanchili
Georgia Institute of Technology

16.30 – 18.00 **COFFEE BREAK AND POSTER SESSION**

STORM: A Simple Traffic-Optimized Router Microarchitecture for Networks-on-Chip
Shalimar Rasheed, Paul Gratz, Srinivas Shakkottai, Jiang Hu

Texas A&M University

Hermes: Architecting a Top-Performing Fault-Tolerant Routing Algorithm for Networks-on-Chips
Vassos Soteriou[1], Costas Iordanou[1], Konstantinos Aisopos[2], Elena Kakoulli[1]
[1]Cyprus University of Technology [2]Microsoft Corporation, USA

Scalability-Oriented Multicast Traffic Characterization
Sergi Abadal[1], Raúl Martínez[2], Eduard Alarcón[1], Albert Cabellos-Aparicio[1]
[1]N3Cat at Universitat Politècnica de Catalunya (UPC) [2]Intel Labs Barcelona

An OFDMA Based RF Interconnect for Massive Multi-core Processors
Eren Unlu[1], Christophe Moy[1], Mohamad Hamieh[2], Myriam Ariaudo[2], Yves Louet[1], Emmanuelle Bourdel[2], Frédéric Drillet[2], Alexandre Briere[3], Julien Denoulet[3], Andréa Pinna[3], Lounis Zerioul[2], Bertrand Granado[3], Patrick Garda[3], François Pêcheux[3], Cédric Duperrier[2], Sébastien Quintanel[2], Olivier Romain[2]
[1]Supelec-IETR [2]ENSEA [3]LIP6

The Connection-Then-Credit Flow Control Protocol for Networks-On-Chips: Implementation and Performance Analysis
Mohamed Sallam[1], M. Watheq El-Kharashi[2], Mohamed Dessouky[3]
[1]Ain-Shams University, Cairo [2]University of Victoria [3]Mentor Graphics, Cairo

CHARM: A Low-Cost Congestion-Aware and Highly Adaptive Routing Method for 2D and 3D On Chip Networks
Manoj Kumar[1], Manoj Singh Gaur[1], Vijay Laxmi[1], Masoud Daneshtalab[2], Pankaj Kumar[1], Seok-Bum Ko[3], Mark Zwolinski[4]
[1]Malaviya National Institute of Technology, Jaipur [2]University of Turku
[3]University of Saskatchewan [4]University of Southampton

Design Trade-offs in Energy Efficient NoC Architectures
Antonis Psathakis, Vassilis Papaefstathiou, Manolis Katevenis, Dionisios Pnevmatikatos
FORTH-ICS

Effective Abstraction for Response Proof of Communication Fabrics
Sayak Ray, Sharad Malik
Princeton University

DyAFNoC: Characterization and Analysis of a Dynamically Reconfigurable NoC using a DOR-based Deadlock-Free Routing Algorithm
Ernesto Cristopher Villegas Castillo, Gabriele Miorandi, Wang Jiang Chau
University of Sao Paulo

An Energy-Efficient Millimeter-Wave Wireless NoC with Congestion-Aware Routing and DVFS
Ryan Kim, Jacob Murray, Paul Wettin, Partha Pande, Behrooz Shirazi
Washington State University

18.00 CLOSING

19.30 SOCIAL EVENT AT THE MEDIEVAL CASTLE OF FERRARA

FRIDAY, SEPTEMBER 19TH, 2014

09.00 – 10.00 KEYNOTE ADDRESS
SpinNNaker: the World's Biggest NoC
Steve Furber - University of Manchester (UK)

10.00 – 11.00 PAPER SESSION 6
FAULT TOLERANCE AND RELIABILITY

6.1 DiAMOND: Distributed Alteration of Messages for On-Chip Network Debug
Rawan Abdel-Khalek, Valeria Bertacco
University of Michigan

6.2 ElastiNoC: A Self-Testable Distributed VC-based Network-on-Chip Architecture
Ioannis Seitanidis[1], Anastasios Psarras[1], Emmanouil Kalligeros[2], Chrysostomos Nicopoulos[3], Giorgos Dimitrakopoulos[1]
[1]Democritus University of Thrace [2]University of the Aegean [3]University of Cyprus

11.00 – 11.30 COFFEE BREAK

11.30 – 13.00 PAPER SESSION 7
NoC ARCHITECTURE III

7.1 Using Packet Information for Efficient Communication in NoCs
Prasanna Venkatesh Rengasamy and Madhu Mutyam
IIT Madras

7.2 A Loosely Synchronizing Asynchronous Router for TDM-Scheduled NOCs
Ioannis Kotleas[1], Dean Humphreys[1], Rasmus Bo Sørensen[1], Evangelia Kasapaki[1], Florian Brandner[2], Jens Sparsø[1]
[1]Technical University of Denmark [2]ENSTA ParisTech, France

7.3 ICARO: Congestion Isolation in Networks-On-Chip
Jose Vicente Escamilla Lopez[1], Josè Flich[1], Pedro Javier Garcia[2]
[1]Universitat Politècnica de València [2]Universidad de Castilla-La Mancha

13.00 – 13.30 BEST PAPER AWARD AND CLOSING
13.30 LUNCH