International Symposium on Networks-on-Chip

The International Symposium on Networks-on-Chip (NOCS) is the premier event dedicated to interdisciplinary research on on-chip, chip-scale, and multichip package-scale communication technology, architecture, design methods, applications and systems. NOCS brings together scientists and engineers working on NoC innovations and applications from inter-related research communities, including computer architecture, networking, circuits and systems, packaging, embedded systems, co-design, and design automation. Topics of interest include, but are not limited to:

NoC Architecture and Design
- Network architecture (topology, routing, arbitration).
- NoC Quality of Service.
- Timing, synchronous/asynchronous communication.
- Network interface issues.
- NoC design methodologies and tools.
- Mapping of applications onto NoCs.
- Signaling & circuit design for NoC links.

NoC Analysis, Verification and Modeling
- Benchmarking & experience with NoC-based hardware.
- Modeling, simulation, and synthesis of NoCs.
- Verification, debug & test of NoCs.
- Metrics and benchmarks for NoCs.
- Scalable modeling of NoCs.

Novel NoC Technologies
- New physical interconnect technologies, e.g., carbon nanotubes, wireless NoCs, through-silicon, etc.
- NoCs for 3D and 2.5D packages.
- Package-specific NoC design.
- Optical, RF, & emerging technologies for on-chip/inpackage interconnects.

NoC Application
- NoC case studies.
- application-specific NoC designs.
- NoC designs for heterogeneous many-core systems, fused CPU-GPU architectures, FPGA-based systems,… etc.

NoC at the Un-Core and System-level
- Design of memory subsystem (un-core) including memory controllers, caches, cache coherence protocols & NoCs.
- NoC support for memory and cache access.
- OS support for NoCs.
- Programming models including shared memory, message passing and novel models.
- Issues related to large-scale systems (datacenters, supercomputers) with NoC-based systems as building blocks.

NoC Optimization
- for power/energy efficiency.
- for thermal efficiency and dark silicon.
- for dependable architectures.
- for communication efficient algorithms.

Electronic paper submission requires a full paper, up to 8 double-column IEEE format pages, including figures and references. The program committee in a double-blind review process will evaluate papers based on scientific merit, innovation, relevance, and presentation. Submitted papers must describe original work that has not been published before or is under review by another conference at the same time. Each submission will be checked for any significant similarity to previously published works or for simultaneous submission to other archival venues, and such papers will be rejected. Please see the paper submission instructions for details. This year will also include an industrial session on the architecture of future NoC platforms. The objective of this session is to provide a forum for industry leaders to share their experiences and perspectives on the technical challenges facing future platforms and discuss potential solutions. Check the submission page for details on submissions to this session. The session will feature a small number of papers (3-5) covering experiences from industrial design and development.

Proposals for tutorials, special sessions, and panels are also invited. Please see the detailed submission instructions for paper, tutorial, special sessions, and panel proposals at the submission page.

Important Dates
- Abstract registration deadline March 2nd, 2014
- Full paper submission deadline March 10th, 2014
- Proposals for tutorials, special sessions and panels May 8th, 2014
- Notification of acceptance May 9th, 2014
- Final version due June 2nd, 2014
- Industry Session submission deadline March 23rd, 2014

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