High-performance
Energy-efficient NoC Fabrics

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Outline

- Technology Scaling
- NoC Trends
- Recent NoCs
- Intel Research NoCs
- Summary
32nm $\Rightarrow$ 22nm Interconnects

R. Brain, IITC 2009

M8  567
M7  450
M6  338
M5  225
M4  169
M3  113
M2  113
M1  113

Low-k

Cu

C. Jan, IEDM 2012

Pitch (nm)

High Perf CPU

High Density SoC

320-360

240

160

112

90

320-360

240

160

112

90
Client Processor Trend: Integrated Graphics

- Sandy Bridge 32nm client processor with monolithic integrated graphics in 2011
- Up to 4 dual-threaded cores
- Dual channel DDR3 memory controller
- Integrated PCI Express interface

Power and Integration Trends

Two additional cores every year

Total Power
Active Power
Leakage

S. Rusu, ISSCC 2009
On-chip Interconnect Challenges

- Technology scaling creates interconnect bottlenecks in both energy and delay

Source: ITRS Roadmap

Global interconnect without repeaters
Global interconnect with repeaters
Local interconnect (M1,2)
Gate delay (FO4)
Exa-scale On-chip Interconnect Challenges

Proc Element (PE)
INT, DP-FP x +
32KB iCache
64KB L1 SP
0.5 MT Core
Logic
0.1 MT Other

Island (8 PE)
Service Core
1MB L2
PE PE PE PE

Processor Chip (16 Clusters)
Interconnect
8MB Shared LLC
64MB Shared LLC

Cluster (16 Islands)
Interconnect
8MB Shared LLC

Top 500 Supercomputers in the world
Performance exceeding 1EFLOPs

Future data-center processor chips:
> 16+ cores per cluster and  > 16+ clusters per die

S. Borkar, IPDPS 2013
Recent NoC Chips

- IBM Power 8™ in 22 nm
- 12 cores, 3.6TB/s total BW
- 150GB/s/direction/core

- KAIST NoC in 130 nm
- 9x10 star + 7x7 xbar ring
- 118 Gb/s NoC

- Tilera TILE64™ in 90 nm
- 64 cores, 5 x 32b mesh
- 120GB/s/tile bandwidth

- UCDavis AsAP2: 167 cores in 65nm
- Statically circuit-switched with source-synchronous handshaking
Intel On-Chip Fabrics

- Ivytown Xeon Processor
  - 15 cores, ring interconnect, 1.2TB/s

- Haswell processor
  - Ring-based interconnect for cache /core + graphics + system agent

- Poulson Itanium Processor
  - 8 cores, ring interconnect, 700GB/s

- Knights Corner Xeon Phi
  - >50 cores, ring interconnect
Outline

• Technology Scaling
• NoC Trends
• Recent NoCs

• Intel Research NoCs
  • 24-node 45nm packet-switched NoC
  • 64-node 45nm circuit-switched NoC
  • 256-node 22nm source-synchronous circuit-switched NoC

• Summary
24-node 45nm Packet-Switched NoC

<table>
<thead>
<tr>
<th>Technology</th>
<th>45nm Hi-K CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interconnect</td>
<td>9 Metal (Cu)</td>
</tr>
<tr>
<td>Transistors</td>
<td>Die: 1.3B, Tile: 48M</td>
</tr>
<tr>
<td>Tile Area</td>
<td>18.7mm²</td>
</tr>
<tr>
<td>Die Area</td>
<td>567.1mm²</td>
</tr>
</tbody>
</table>

J. Howard, ISSCC 2010
P. Salihundam, JSSC 2011
Router Architecture and Pipeline

Port 0

Port 1 to 4

24-deep flit FIFO

WEST NORTH EAST SOUTH LOCAL

Port 0

STAGE 1
Link Traversal + Buffer Write

STAGE 2
Switch Allocation

STAGE 3
Buffer Read + VC Allocation

STAGE 4
Switch Traversal

Crossbar

Switch Arbitration

Clk

8 VCs over 2 Message classes

4 cycle no-load latency
Total Power | 550mW/router, 13.2W total at 1.1V, 2GHz and 50°C
Standby Power | 68mW at 1.1V and 50°C
Transistors | 640K
Area | 1.17mm²
• Fully synchronous packet switching has high overhead:
  • Global clock distribution and clock-crossing synchronizers
  • Packet storage in routers with multi-cycle latency
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• Summary
- Circuit-switched NoC eliminates intra-route data storage
- Packet-switching used only for channel requests
  ⇒ High bandwidth and energy efficiency
Request Packet Transmission

- Request packet X to be sent from core (0,0) to core (2,1)
- Moves one core during each PCI cycle
- Inport determines direction
- Outport chooses which packet to send
• Request packet X leaves trail of routing direction
• Trail allocates resources, blocks later packets along path
Request Packet Arrival

- Request packet X arrives at destination, ready for ack
Acknowledge Phase

- Allocated path forwards acknowledge to transmitter
- Full CClk cycle for sending acknowledge
- Indicates to transmitter that path is available next cycle
Circuit-switched Data Transmission

- Next CClk cycle, data is sent on allocated path
- Simultaneous acknowledges for next data path
- No flip-flops along entire path, only repeaters and muxes
- Path automatically released at end of CClk cycle
Channel Selection and Transmission

- Queue slots store multiple channel requests
- Two acknowledges required to indicate ready channel
- More possible channels ⇒ 87% throughput increase
- Channel directions stored in 8x2b register file
- Selected slot reads channel direction from register file
- 63% reduced slot select delay vs. linear search
Streaming Data Transmission

- Multiple data transfers per channel allocation
- DCIk and SCIk trigger data transmission and capture
- Proximity-based streaming increases throughput 4.5X
8x8 NoC Die Micrograph

<table>
<thead>
<tr>
<th>Process</th>
<th>45nm Hi-K/MG CMOS, 9 Metal Cu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal Supply</td>
<td>1.1V</td>
</tr>
<tr>
<td>Arbitration and Router Logic</td>
<td>Supports 512b data</td>
</tr>
<tr>
<td>Number of Transistors</td>
<td>2.85M</td>
</tr>
<tr>
<td>Die Area</td>
<td>6.25mm²</td>
</tr>
</tbody>
</table>
Traffic Measurements

- 45nm CMOS, 1.1V, 50°C, Random Traffic
- Random traffic power/router: 21mW – 74mW
- Maximum random traffic throughput 2.64Tb/s with 4.73W
- Low traffic power of 1.35W
Arbitration power drops from 17% at 1.1V to 10% at 550mV
Low voltage operation improves efficiency to 1.51Tb/s/W
Traffic Measurements

- Maximum throughput traffic energy efficiency: 3.0Tb/s/W
- Maximum power traffic energy efficiency: 0.51Tb/s/W
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• Summary
16x16 22nm NoC Organization

G. Chen, ISSCC 2014

- Source-synchronous operation reduces clock power
- Supports design heterogeneity and delay variations
Source-Synchronous Operation

- Forwarded clock sent with each transfer
- Delay-adaptive for multiple voltage/clock domains
- Delay averaging for resilience to process variation
Hybrid Packet/Circuit Switching

- Packet-switched requests reserve circuit channels
- Circuit-switched data with no intra-route storage
- Ack indicates completed transfer
NoC Operation

- Request packet with single pipeline stage per router
- Credit tracking controls the request packet pipeline
NoC Operation

- FIFO queues channel setup direction
- Request packets propagate ahead of circuit transfer
• Direction configures circuit-switched channel
• Circuit transfer occurs without intra-route storage
Streaming amortizes channel setup energy
Tail Ack deallocates circuit-switched channel
Credit Tracking Circuits

- Credit-2 removes round-trip latency between routers
- Improves packet throughput by 89%
Credit Tracking Circuits

- Latency set by exercised instead of worst-case path
- Improves packet throughput by 35%
Credit Tracking Circuits

- Credit tracking with single C-element
- Handles arbitrary arrival of Request and Grant
Packet Direction Circuits

- 32b sideband improves throughput by 72%
- Input latches block packet when router is busy
- Double-edge flip-flop reduces clock power by 25%
Channel Reservation Operation

- Packets store direction for later channel setup
- Requests cleared after circuit transfer completion
- Hides request packet delay for 62% lower latency
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Channel Reservation FIFO

- 3b Gray-counter pointers prevent glitching
- Handles unpredictable signal arrival times
- 4 FIFO entries improve throughput by 75%
• Direction from FIFO configures channel multiplexers
• Path-specific delay for 93% latency reduction
# 16x16 NoC Die Micrograph

![16x16 NoC Die Micrograph](image)

<table>
<thead>
<tr>
<th>Process</th>
<th>22nm Tri-gate CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal Supply</td>
<td>0.9V</td>
</tr>
<tr>
<td>Number of Transistors</td>
<td>150M</td>
</tr>
<tr>
<td>Testchip/Equivalent NoC Area</td>
<td>21.5mm² / 167mm²</td>
</tr>
<tr>
<td>Router Area</td>
<td>138µm x 109µm</td>
</tr>
<tr>
<td>Data Bus Width</td>
<td>112b (80b Circuit/32b Packet)</td>
</tr>
<tr>
<td>Interconnect Length</td>
<td>855µm</td>
</tr>
</tbody>
</table>
Insertion Interval Measurements

- 32b packet-switched energy efficiency 4.48Tb/s/W
- Circuit switching improves energy efficiency by 55%

22nm CMOS, 0.9V, 25°C
Max Throughput
Traffic

Energy Efficiency (Tb/s/W)

Packet

Stream

Circuit 10B

Circuit 128B

Circuit 1kB

0 1 10 100 1000 10000
Insertion Interval (ns)
Latency Measurements

- Delay averaging for 14% packet latency reduction
- Proximity-based delay for 93% lower circuit delay
- 62% faster circuit transfer vs. packet transfer

22nm CMOS, 0.9V, 25°C

Latency Measurements

- Delay averaging for 14% packet latency reduction
- Proximity-based delay for 93% lower circuit delay
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22nm CMOS, 0.9V, 25°C
• Source-sync removes clock and synchronization overhead
• Hybrid switching eliminates flip-flop power
• Approach the power of a point-to-point connection
Summary

• Industry SoCs are evolving from buses or crossbars toward 2D meshes
• Both high performance and energy efficiency important as NoC size grows
• Future SoCs will have varying network constraints and requirements
  • No single network will be optimal
  • Multiple hierarchical, heterogenous NoCs
  • Resiliency to variations and faults
• Exascale communication power expected to far exceed computation power
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