Call for Papers

The AISTECS workshop is the 4th edition of successfully blending the INA-OCMC workshop (9 editions at HiPEAC, 2007-2015) and the envelope-pushing Silicon Photonics workshop (2 editions at HiPEAC, 2014-2015) into one. The AISTECS workshop promotes research and knowledge exchange on advanced interconnect designs leveraging emerging technologies to support a wide variety of computing platforms ranging from high-performance computing systems and datacenters down to embedded and Internet of Things (IoT) devices.

Interconnects are subject to growing expectations in terms of performance and Quality of Service while being tied to shrinking power and cost budget, as well as thermal envelopes. Addressing this outstanding challenge requires the identification and solving of crucial design challenges in the pathway to enabling the widespread adoption of effective interconnects in next-generation computing platforms. Novel interconnects, thanks to their potential disruptive properties, may also disrupt the expected shape of future computer systems from both the design and programmability viewpoints.

The workshop aims to gather a complete range of perspectives, spanning from raw technology issues and solutions up to studies at the overall system level of modern multi-/many-core systems. This encompasses novel network solutions from both academic and industrial researchers.

Important Dates
Submission deadline: November 23rd, 2018 (11h59p AoE – anywhere on earth)
Author notification: December 8th, 2018
Camera-ready paper due: December 22nd, 2018

Submission Format and Website
AISTECS welcomes both short work-in-progress articles describing breaking new ideas, as well as full papers with more mature evaluations. All papers will undergo a single-blind peer review process, emphasizing novelty/potential in the work-in-progress submissions and implementation/evaluation in the full paper submissions. Presentation times will be allocated according to the type of paper.

Work-in-progress papers are limited to 2 pages, whereas full papers are limited to 4 pages (A4). All articles must be formatted in accordance to the ACM two-column style (https://www.acm.org/publications/proceedings-template), including title, authors, affiliations and corresponding author email. Papers deviating significantly from the paper size and formatting rules may be rejected without review.

Papers must be submitted in PDF format via EasyChair (https://easychair.org/conferences/?conf=aistecs2019).

Workshop Topics
Emerging Interconnect Technologies
- Silicon photonics, wireless, and RF
- Carbon nanotubes, through-silicon vias, near-field coupling interconnects
- NoCs for 3D and 2.5D packages, including interposer-based systems

Reliability and Security
- Reliability, availability, fault tolerance for system communication
- Fault-tolerant routing, approximate NoCs
- Secure intra-chip and inter-chip communication, mitigation of hardware trojan effects

Performance, Power, Energy and Thermal Issues
- Benchmarks, simulation, performance and Quality of Service (QoS) management
- Thermal-/energy-and power-related NoC optimization and dark silicon
- Thermal-aware designs in silicon photonics and 3D NoCs
Impact of the interconnect on application performance
Network solutions for performance isolation in many-cores

NoC Architecture and Implementation
- Topologies, routing, flow control
- Synchronous/asynchronous interconnects
- Design methodologies and tools
- Signaling & circuit design for NoC links

Interconnect Design for Memory Subsystems
- Memory interconnect and coherence support
- NoC support for memory and cache access
- Programming models for shared memory, message passing and novel programming models

Internet of Things, High Performance Computing and GPUs
- Interconnect solutions for heterogeneous GPU/FPGA-based multi/macro-chip systems
- Communication infrastructures for HPC systems, Supercomputers and Data Centers
- Reconfigurable/programmable interconnect components
- Interconnect architectures for neuromorphic computing
- Network infrastructures for Internet-of-Things devices

Registration
At least one registration is required per accepted paper, and one author is expected to present the paper at the workshop. Registration will be handled via the HiPEAC Conference.

Publication
(To be confirmed) Accepted papers will be published in the ACM Digital Library within the ACM International Conference Proceedings Series (ICPS). Authors will be sent the ACM form and instructions to finalize the camera-ready submission and to complete the publication procedure.

Workshop Organizers
GENERAL CHAIRS:
- Sören Sonntag, Intel, Germany
- Davide Bertozzi, University of Ferrara, Italy

PROGRAM CHAIRS:
- Sergi Abadal, Universitat Politècnica de Catalunya, Spain
- Davide Zoni, Politecnico di Milano, Italy

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- Cyriel Minkenberg, Rockley Photonics, USA
- Sören Sonntag, Intel, Germany
- Davide Bertozzi, University of Ferrara, Italy

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- Tushar Krishna, Georgia Tech, USA
- Sébastien Le Beux, Lyon Institute of Nanotechnology, France
- Sergei Mingaleev, VPIphotonics, Germany
- Daniel Müller-Gritschneder, TU Munich, Germany
- Chrysostomos Nicopoulos, University of Cyprus, Cyprus